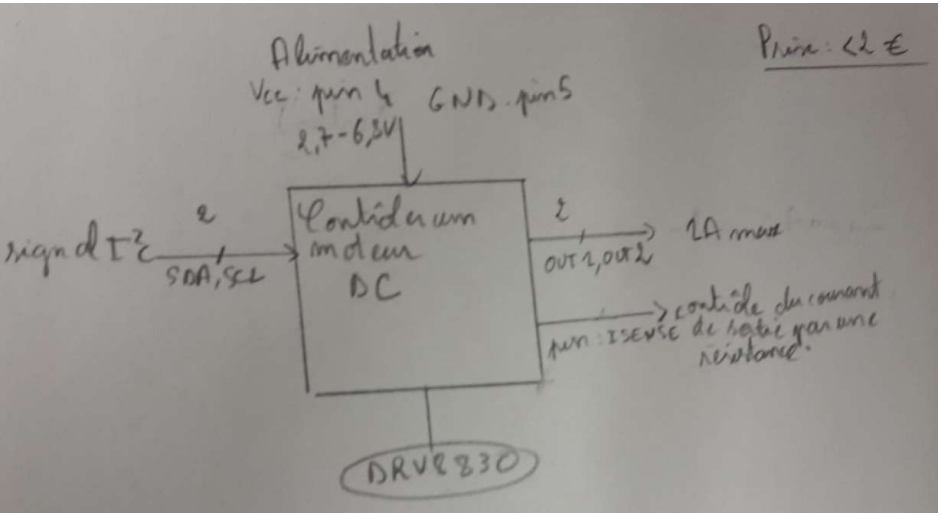
Circuit intégré pour contrôler moteur courant continu: DRV8830



8.2 Typical Application

Figure 11 is a common application of the DRV8830.

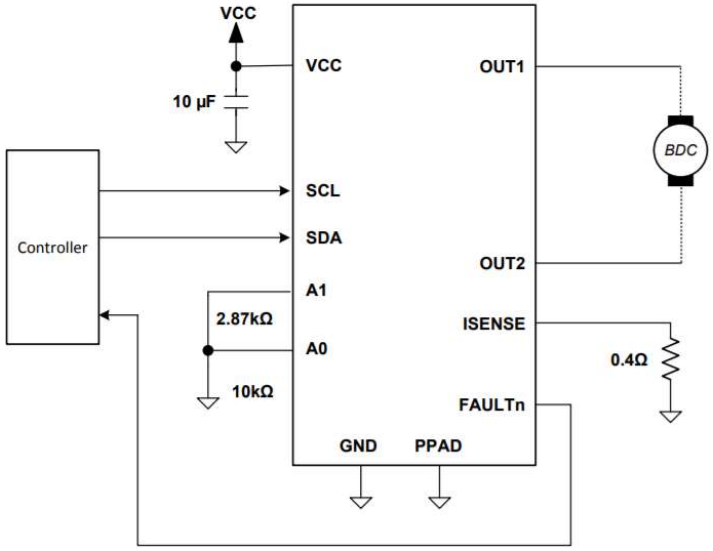
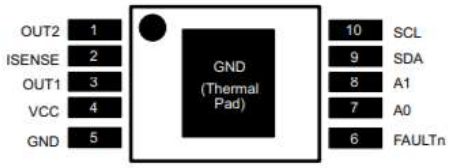


Figure 11. Motor Control Circuitry

DGQ or DRC Package
10-Pin HVSSOP or VSON
Top View



The HVSSOP package has a PowerPAD.

Pin Functions

PIN		TYPE(1)	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NO.			
A0	7	I	Address set 0	Connect to GND, VCC, or open to set I²C base address. See serial interface description.
A1	8	I	Address set 1	
FAULTn	6	OD	Fault output	Open-drain output driven low if fault condition present
GND	5	—	Device ground	
ISENSE	2	IO	Current sense resistor	Connect current sense resistor to GND. Resistor value sets current limit level.
OUT1	3	O	Bridge output 1	Connect to motor winding
OUT2	1	O	Bridge output 2	
SCL	10	I	Serial clock	Clock line of I²C serial bus
SDA	9	IO	Serial data	Data line of I²C serial bus
VCC	4	—	Device and motor supply	Bypass to GND with a 0.1-µF (minimum) ceramic capacitor.

(1) Directions: I = input, O = output, OZ = tri-state output, OD = open-drain output, IO = input/output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
VCC	Power supply voltage	–0.3	7	V
	Input pin voltage	–0.5	7	V
	Peak motor drive output current(3)	Internally limited		A
	Continuous motor drive output current(3)	–1	1	A
	Continuous total power dissipation	See *Thermal Information*		
T_J	Operating virtual junction temperature	–40	150	°C
T_{stg}	Storage temperature	–60	150	

10.2 Layout Example

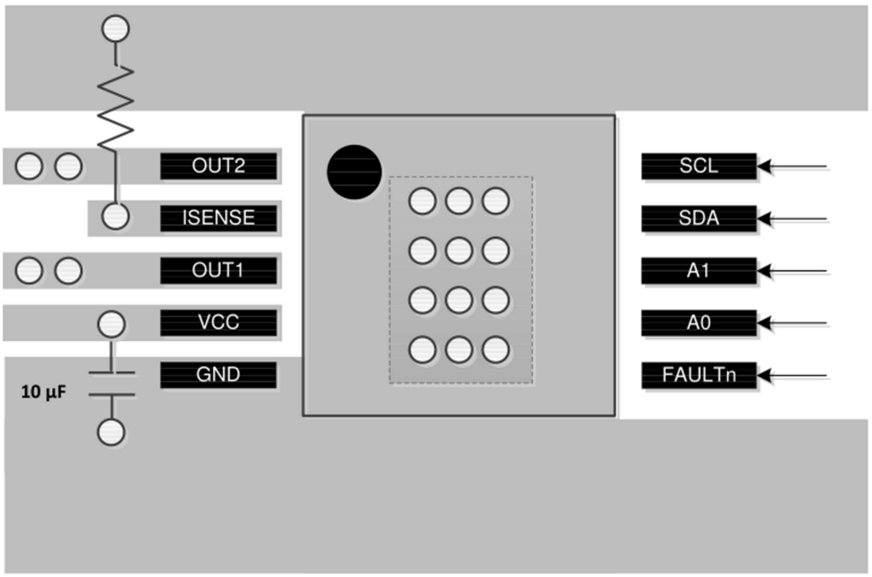
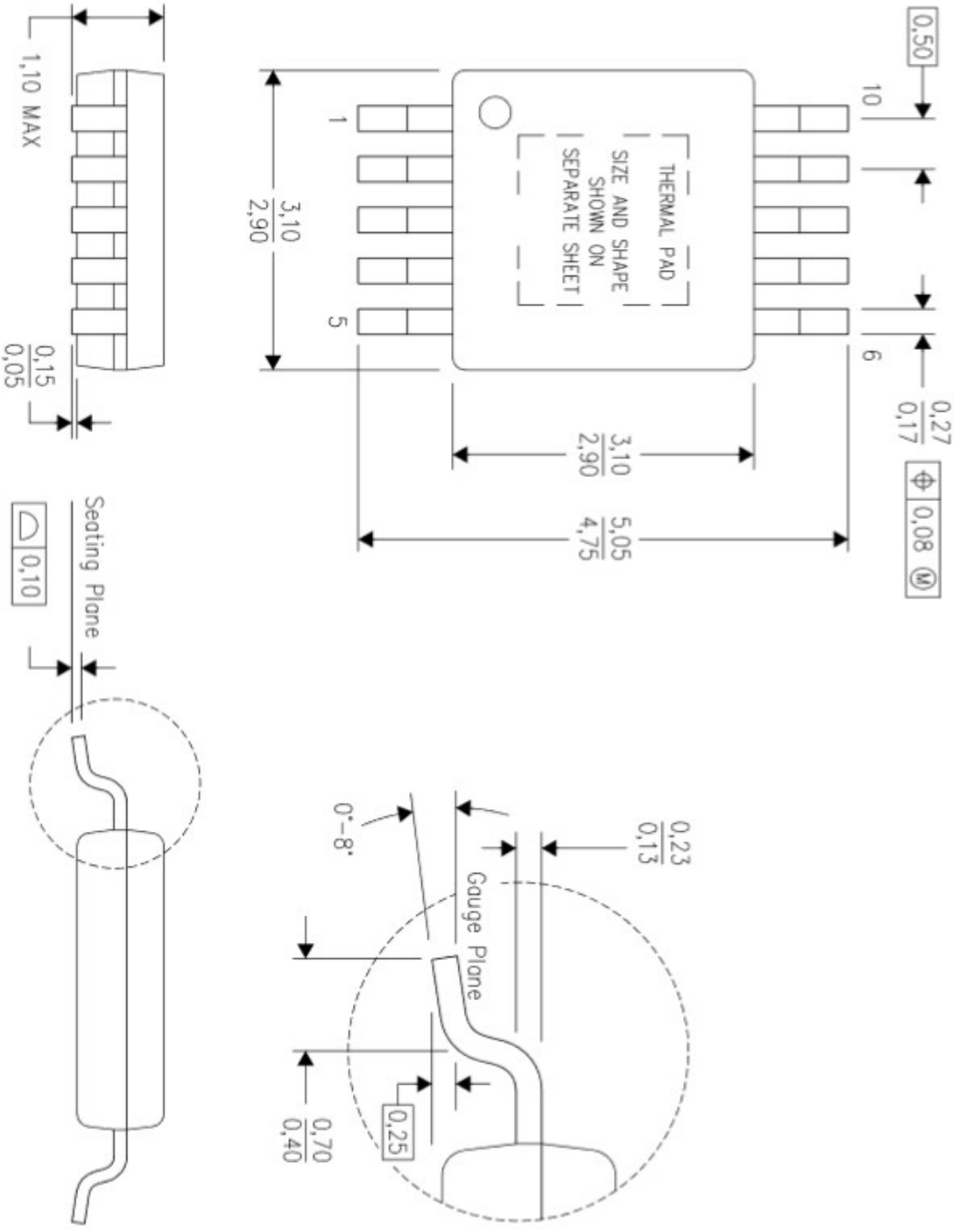
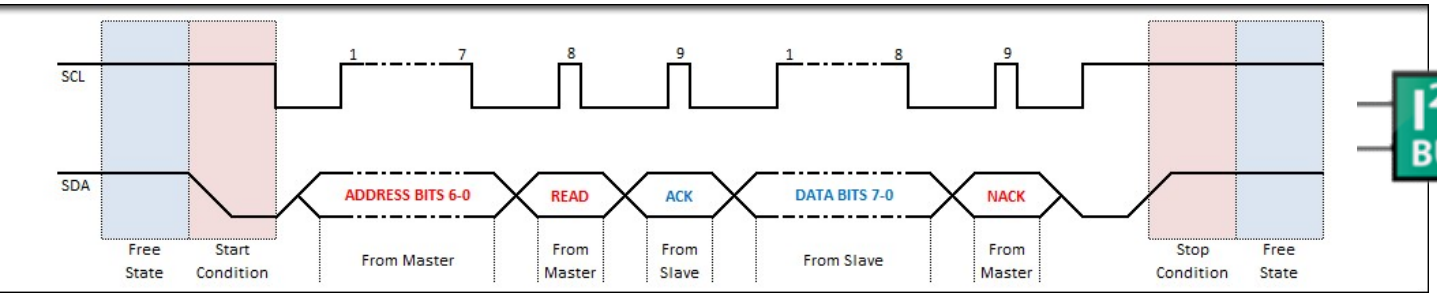
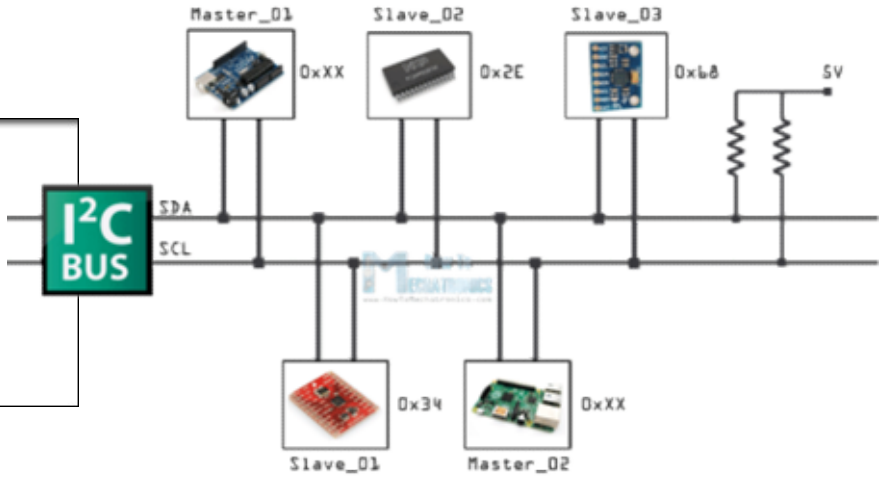


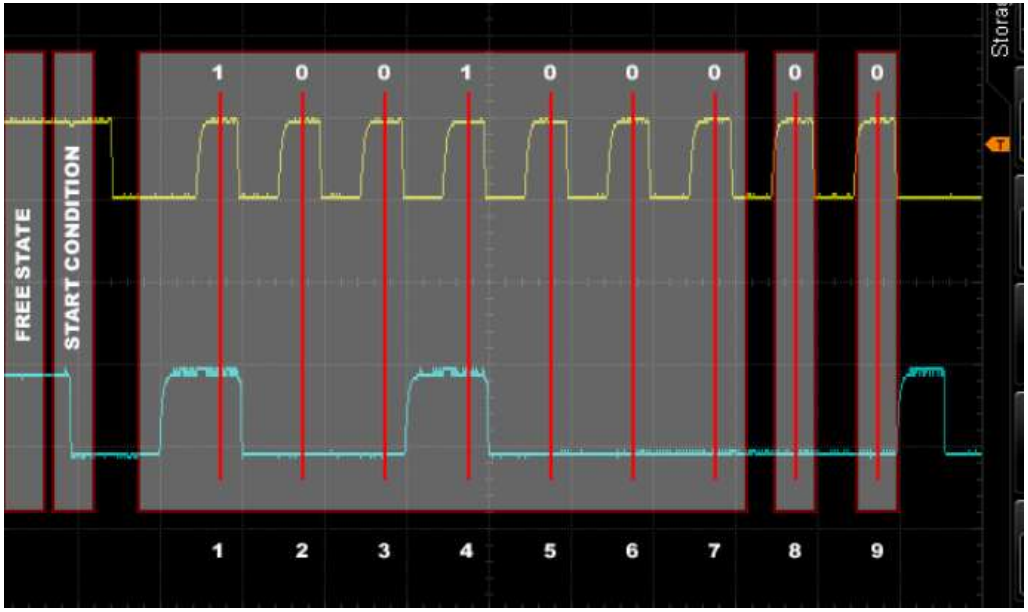
Figure 18. Layout Recommendation



I2C: Two wires for all (as opposed to SPI)







I2C: Two wires for all (as opposed to SPI)

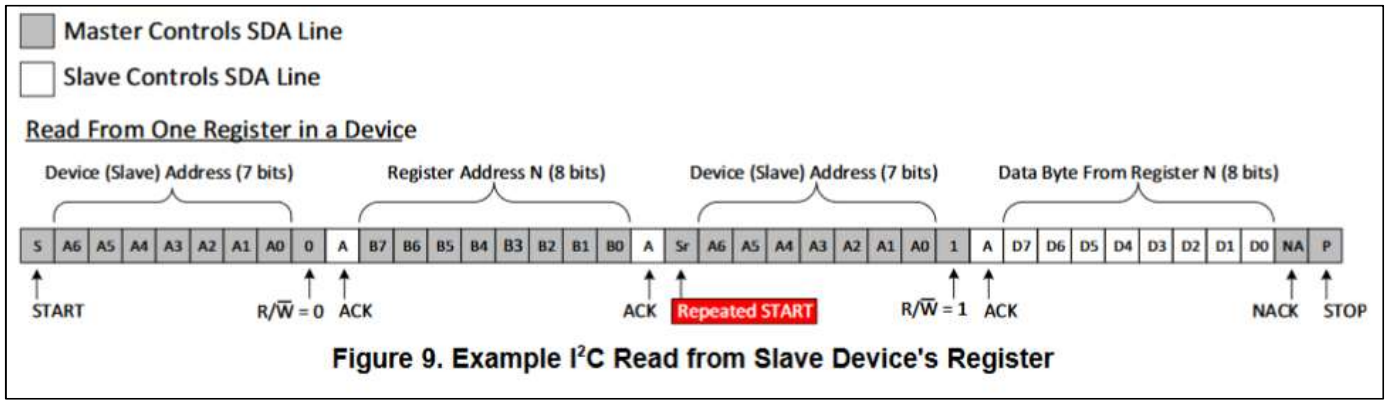


Figure 9. Example I²C Read from Slave Device's Register

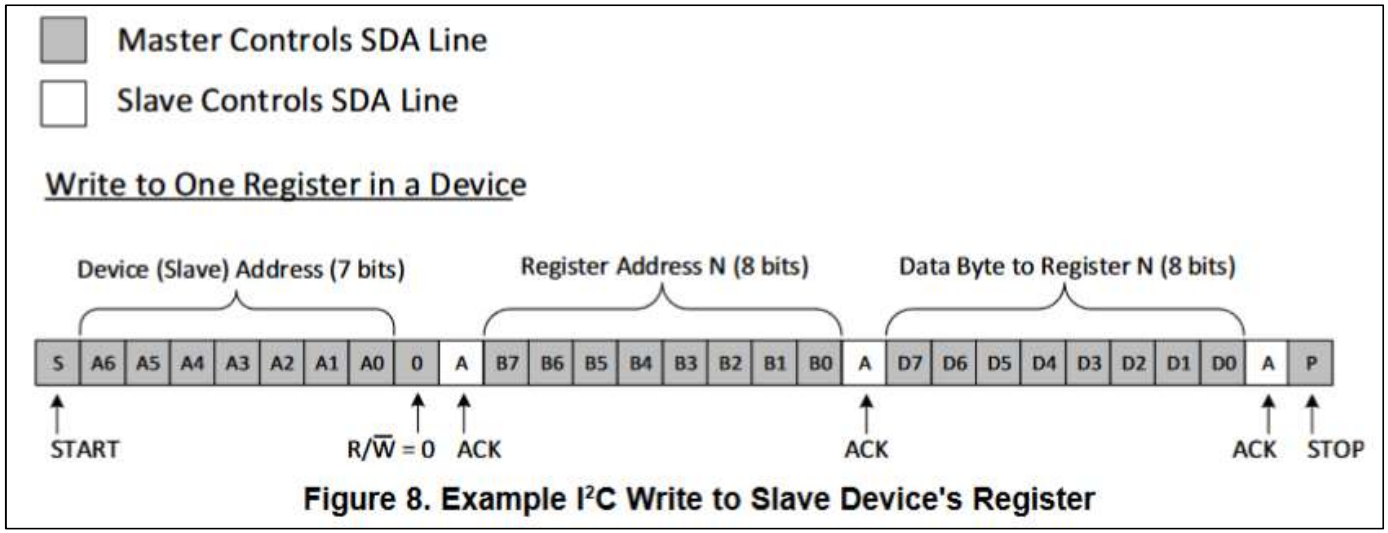


Figure 8. Example I²C Write to Slave Device's Register

ARDUINO

Wire Library

Functions

- begin()
- requestFrom()
- beginTransmission()
- endTransmission()
- write()
- available()
- read()
- SetClock()
- onReceive()
- onRequest()

DRV8830 I2C

The upper address bits of the device address are fixed at 0xC0h, so the device address is as follows:

Table 5. Device Addresses

A1 PIN	A0 PIN	A3..A0 BITS (as below)	ADDRESS (WRITE)	ADDRESS (READ)
0	0	0000	0xC0h	0xC1h
0	open	0001	0xC2h	0xC3h
0	1	0010	0xC4h	0xC5h
open	0	0011	0xC6h	0xC7h
open	open	0100	0xC8h	0xC9h
open	1	0101	0xCAh	0xCBh
1	0	0110	0xCCh	0xCDh
1	open	0111	0xCEh	0xCFh
1	1	1000	0xD0h	0xD1h

The DRV8830 does not respond to the general call address.

A data byte follows the address acknowledge. If the R/W bit is low, the data is written from the master. If the R/W bit is high, the data from this device are the values read from the register previously selected by a write to the subaddress register. The data byte is followed by an acknowledge sent from this device. Data is output only if

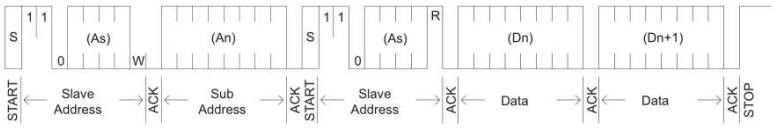


Figure 9. I²C Read Mode

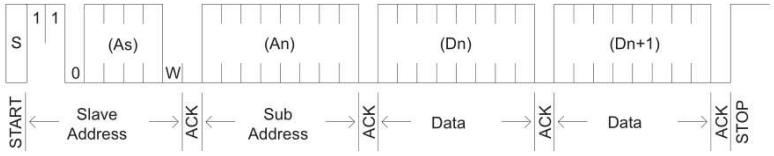


Figure 10. I²C Write Mode

7.6 Register Maps

7.6.1 I²C Register Map

Table 6. I²C Register Map

REGISTER	SUB ADDRESS (HEX)	REGISTER NAME	DEFAULT VALUE	DESCRIPTION
0	0x00	CONTROL	0x00h	Sets state of outputs and output voltage
1	0x01	FAULT	0x00h	Allows reading and clearing of fault conditions

7.6.1.1 REGISTER 0 – CONTROL

The CONTROL register is used to set the state of the outputs as well as the DAC setting for the output voltage. The register is defined as follows:

Table 7. Register 0 – Control

D7 - D2	D1	D0
VSET[5..0]	IN2	IN1

Table 4. H-Bridge Logic

IN1	IN2	OUT1	OUT2	FUNCTION
0	0	Z	Z	Standby / coast
0	1	L	H	Reverse
1	0	H	L	Forward
1	1	H	H	Brake

VSET[5..0]: Sets DAC output voltage. Refer to V

IN2: Along with IN1, sets state of outputs

IN1: Along with IN2, sets state of outputs

Table 1. Commanded Output Voltage (continued)

VSET[5..0]	OUTPUT VOLTAGE	VSET[5..0]	OUTPUT VOLTAGE
0x10h	1.29	0x30h	3.86
0x11h	1.37	0x31h	3.94
0x12h	1.45	0x32h	4.02

7.6.1.2 REGISTER 1 – FAULT

The FAULT register is used to read the source of a fault condition, and to clear the status bits that indicated the fault. The register is defined as follows:

Table 8. Register 1 – Fault

D7	D6 - D5	D4	D3	D2	D1	D0
CLEAR	Unused	ILIMIT	OTS	UVLO	OCP	FAULT

CLEAR: When written to 1, clears the fault status bits

ILIMIT: If set, indicates the fault was caused by an extended current limit event

OTS: If set, indicates that the fault was caused by an overtemperature (OTS) condition

UVLO: If set, indicates the fault was caused by an undervoltage lockout

OCP: If set, indicates the fault was caused by an overcurrent (OCP) event

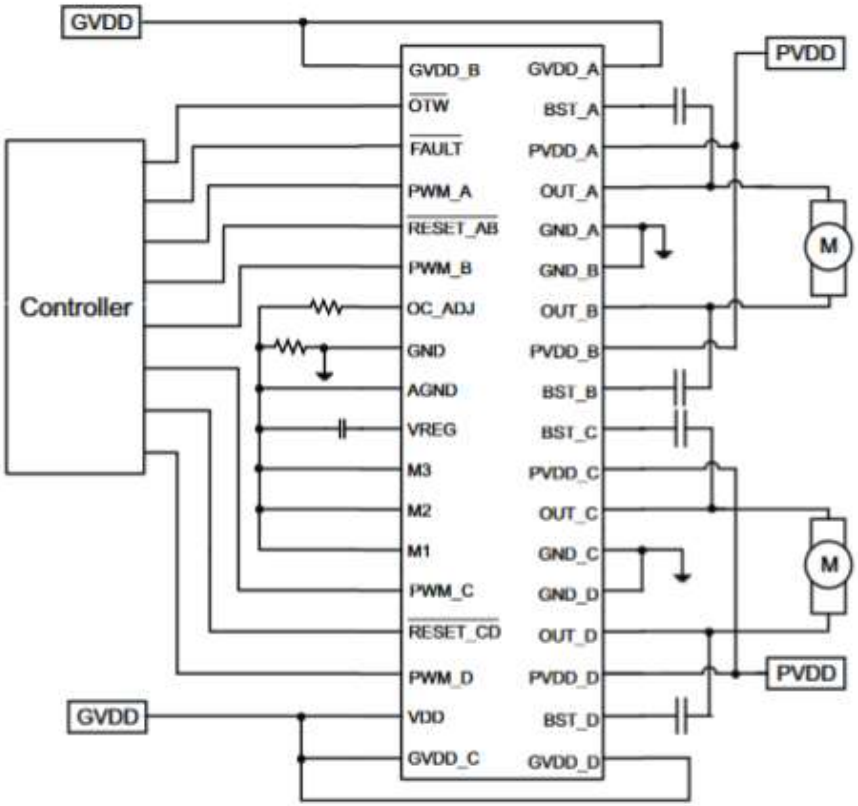
FAULT: Set if any fault condition exists

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8412	HTSSOP (44)	14.00 mm x 6.10 mm
DRV8432	HSSOP (36)	15.90 mm x 11.00 mm

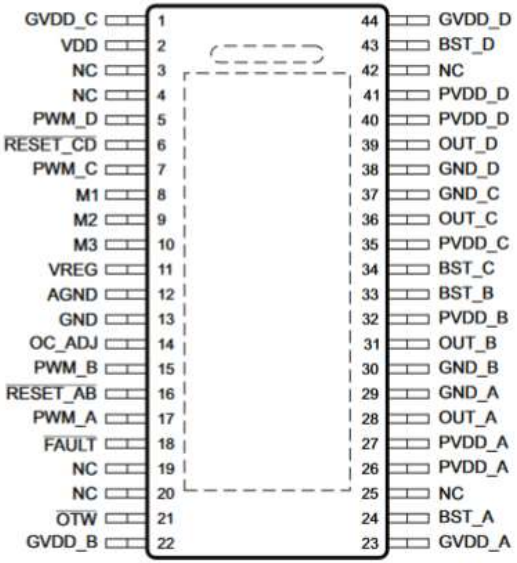
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application Diagram

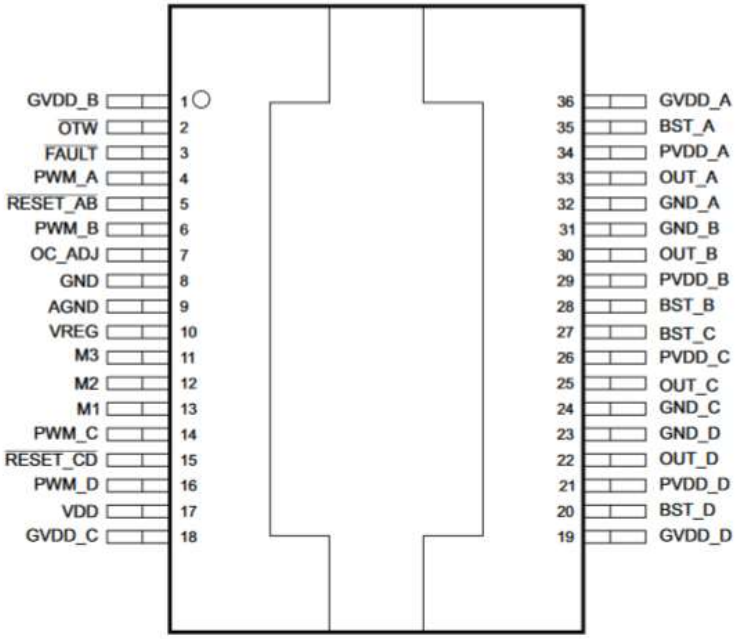


5 Pin Configuration and Functions

DRV8412
DDW Package
(Top View)



DRV8432
DKD Package
(Top View)



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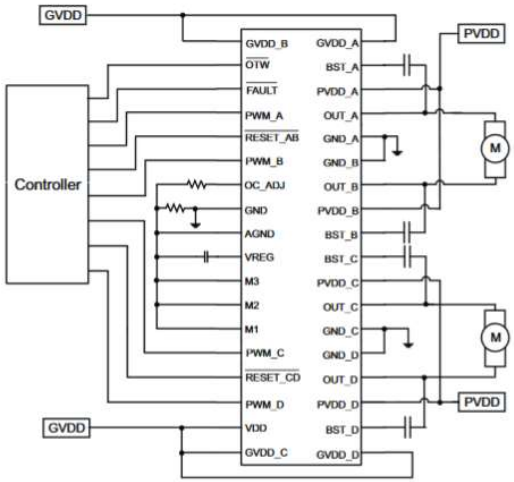
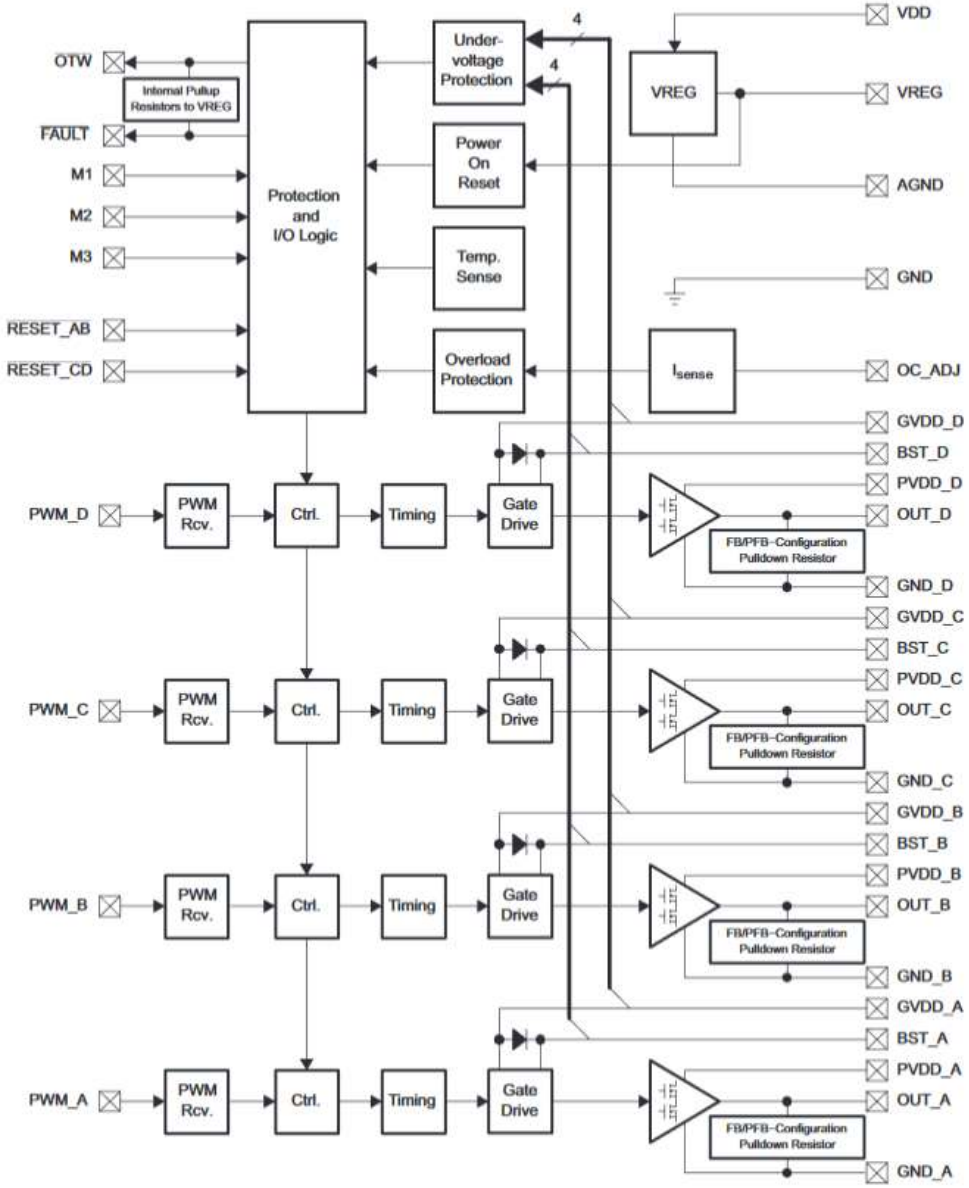
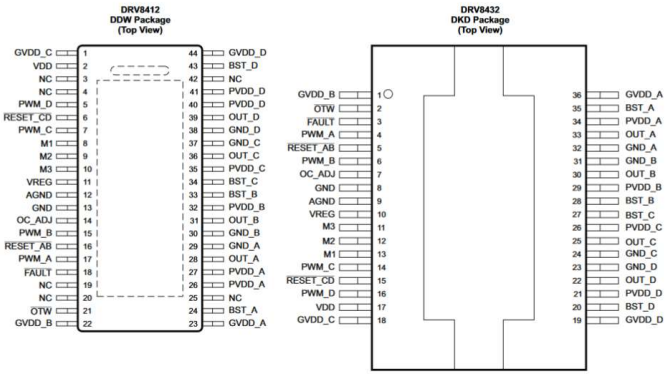


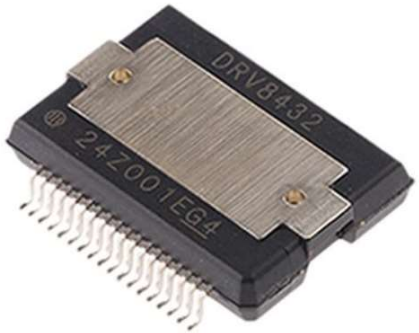
The DRV841x2 requires two power supplies, one at 12 V for GVDD and VDD, and another up to 50 V for PVDD. The DRV841x2 can operate at up to 500-kHz

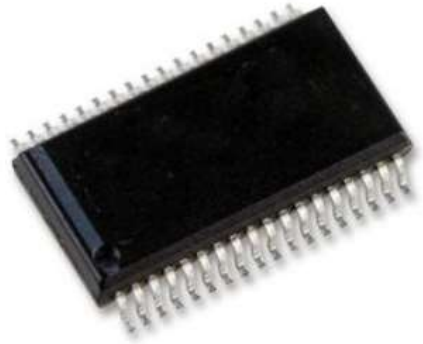
7.2 Functional Block Diagram



5 Pin Configuration and Functions







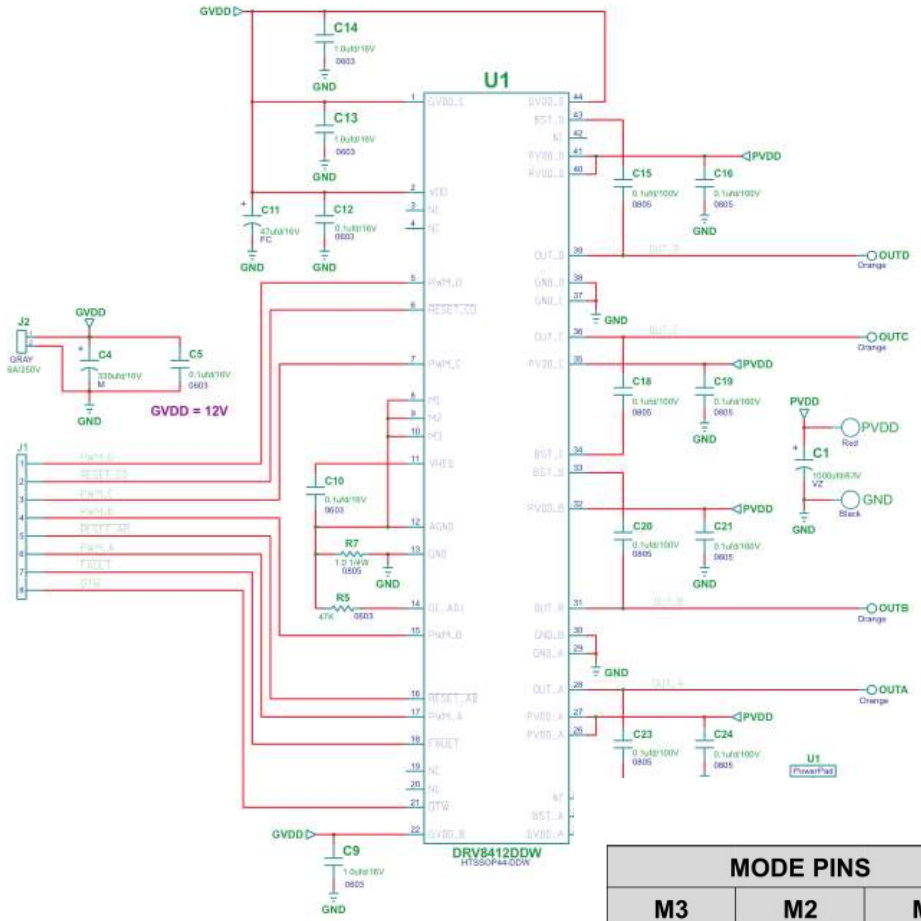
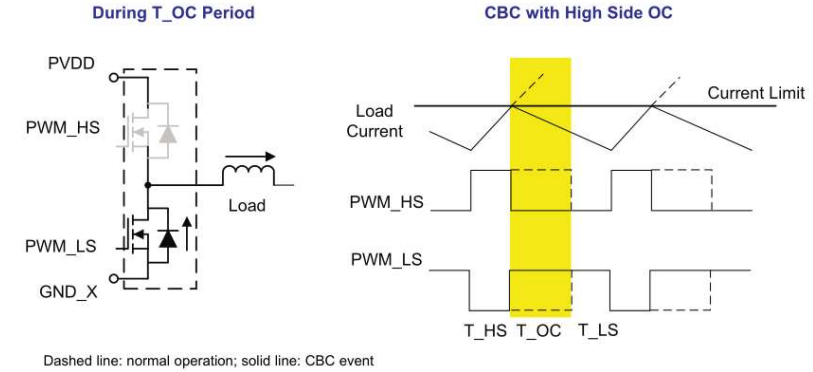
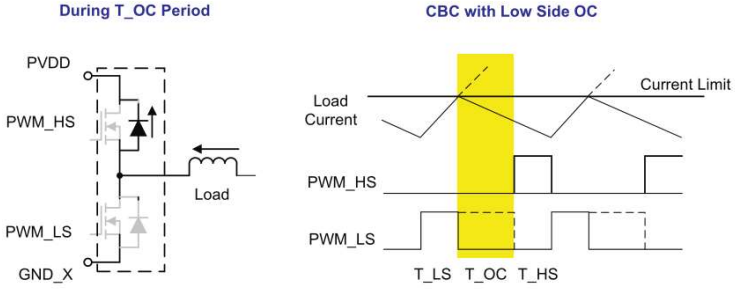


Figure 20. DRV8412 Schematic E:



Dashed line: normal operation; solid line: CBC event

Figure 6. Cycle-by-Cycle Operation With High-Side OC



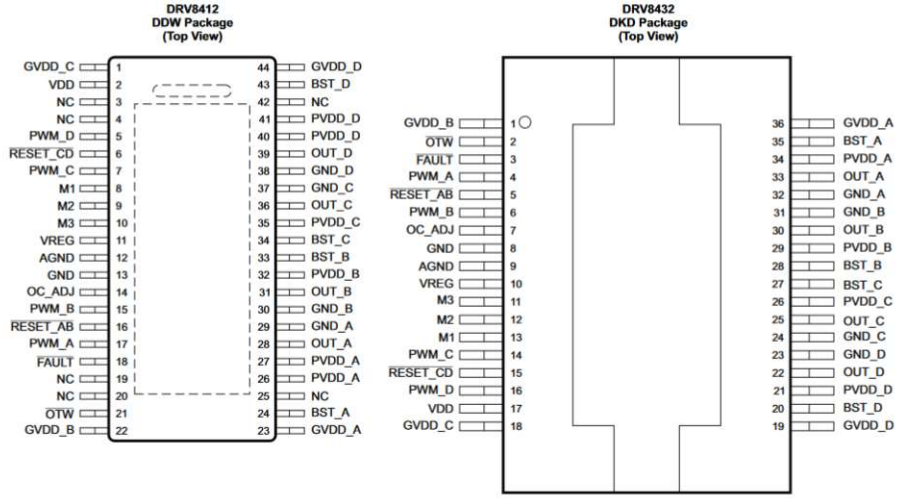
Dashed line: normal operation; solid line: CBC event

Figure 7. Cycle-by-Cycle Operation With Low-Side OC

Mode Selection Pins

MODE PINS			OUTPUT CONFIGURATION	DESCRIPTION
M3	M2	M1		
0	0	0	2 FB or 4 HB	Dual full bridges (two PWM inputs each full bridge) or four half bridges with cycle-by-cycle current limit
0	0	1	2 FB or 4 HB	Dual full bridges (two PWM inputs each full bridge) or four half bridges with OC latching shutdown (no cycle-by-cycle current limit)
0	1	0	1 PFB	Parallel full bridge with cycle-by-cycle current limit
0	1	1	2 FB	Dual full bridges (one PWM input each full bridge with complementary PWM on second half bridge) with cycle-by-cycle current limit
1	x	x	Reserved	

5 Pin Configuration and Functions



AGND	12	9	P	Analog ground
BST_A	24	35	P	High side bootstrap supply (BST), external capacitor to OUT_A required
OC_ADJ	14	7	O	Analog overcurrent programming pin, requires resistor to AGND
$\overline{\text{OTW}}$	21	2	O	Overtemperature warning signal, open-drain, active-low. An internal pullup resistor to VREG (3.3 V) is provided on output. Level compliance for 5-V logic can be obtained by adding external pullup resistor to 5 V
PVDD_D	40, 41	21	P	Power supply input for half-bridge D requires close decoupling capacitor to ground.
PWM_A	17	4	I	Input signal for half-bridge A
GND_D	38	23	P	Power ground for half-bridge D
GVDD_A	23	36	P	Gate-drive voltage supply
$\overline{\text{RESET\_AB}}$	16	5	I	Reset signal for half-bridge A and half-bridge B, active-low
$\overline{\text{RESET\_CD}}$	6	15	I	Reset signal for half-bridge C and half-bridge D, active-low
$\overline{\text{FAULT}}$	18	3	O	Fault signal, open-drain, active-low. An internal pullup resistor to VREG (3.3 V) is provided on output. Level compliance for 5-V logic can be obtained by adding external pullup resistor to 5 V
VDD	2	17	P	Power supply for digital voltage regulator requires capacitor to ground for decoupling.
VREG	11	10	P	Digital regulator supply filter pin requires 0.1-µF capacitor to AGND.
THERMAL PAD	—	N/A	T	Solder the exposed thermal pad to the landing pad on the pcb. Connect landing pad to bottom side of pcb through via for better thermal dissipation. This pad should be connected to GND.
HEAT SLUG	N/A	—	T	Mount heat sink with thermal interface on top of the heat slug for best thermal performance.

Feature Description (continued)

- Ipeak = 15 A (below abs max rating) (1)

Because an inductor usually saturates after reaching its current rating, it is recommended to use an inductor with a doubled value or an inductor with a current rating well above the operating condition.

Table 2. Programming-Resistor Values and OC Threshold

OC-ADJUST RESISTOR VALUES (kΩ)	MAXIMUM CURRENT BEFORE OC OCCURS (A)
22 (1)	11.6
24	10.7
27	9.7
30	8.8
36	7.4
39	6.9
43	6.3
47	5.8
56	4.9
68	4.1
82	3.4
100	2.8
120	2.4
150	1.9
200	1.4

(1) Recommended to use in OC Latching Mode Only

7.3.2.3 Overtemperature Protection

The DRV841x2 has a two-level temperature-protection system that asserts an active-low warning signal ($\overline{OTW}$) when the device junction temperature exceeds 125°C (nominal) and, if the device junction temperature exceeds 150°C (nominal), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and $\overline{FAULT}$ being asserted low. OTSD is latched in this case and $\overline{RESET\_AB}$ and $\overline{RESET\_CD}$ must be asserted low to clear the latch.

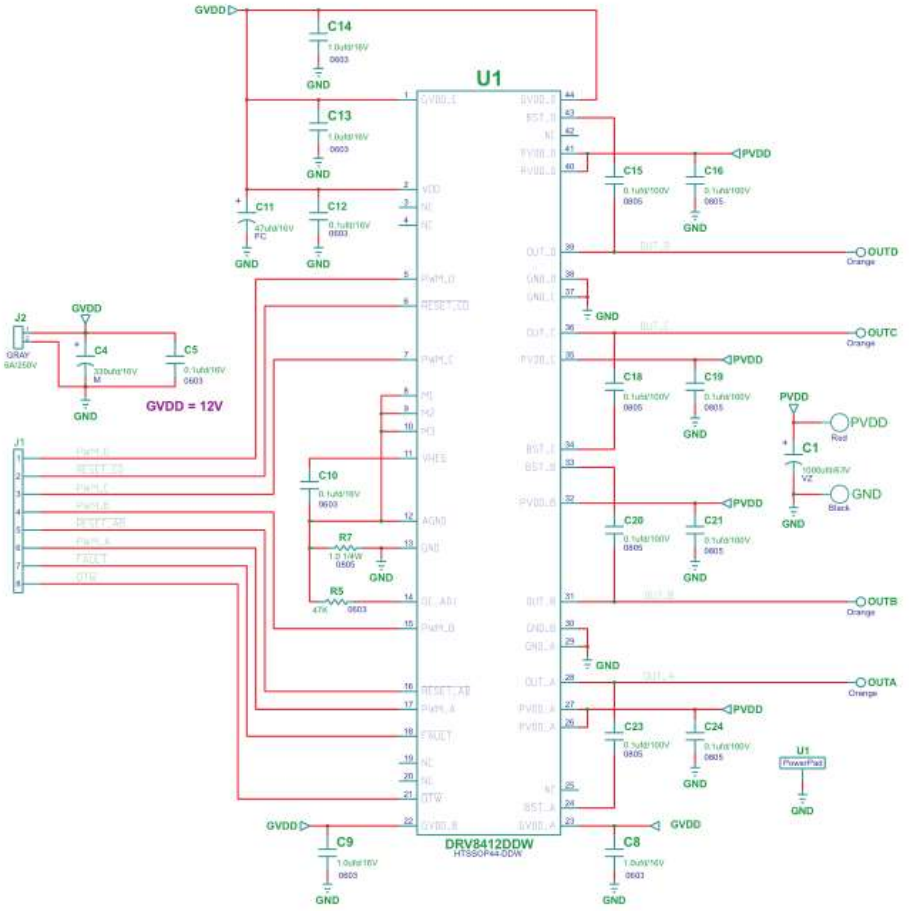


Figure 20. DRV8412 Schematic Example

10.3.1 DRV8412 Thermal Via Design Recommendation

Thermal pad of the DRV8412 is attached at bottom of device to improve the thermal capability of the device. The thermal pad has to be soldered with a very good coverage on PCB in order to deliver the power specified in the datasheet. The figure below shows the recommended thermal via and land pattern design for the DRV8412. For additional information, see TI application report, PowerPad Made Easy (SLMA004) and PowerPad Layout Guidelines (SOLA120).

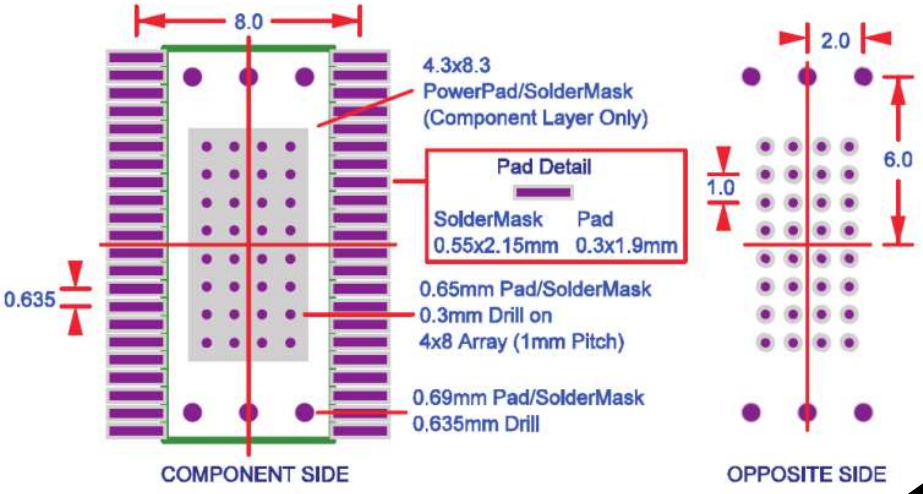
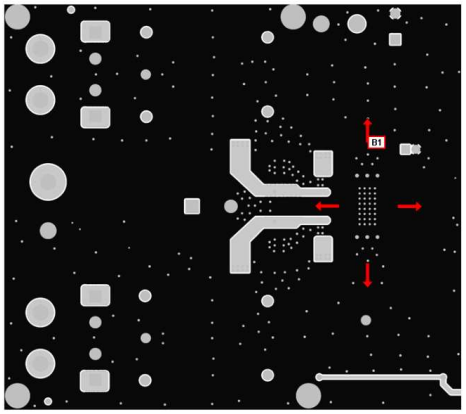
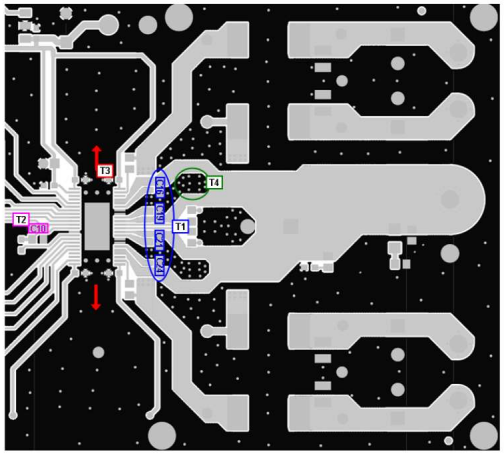


Figure 23. DRV8412 Thermal Via Footprint



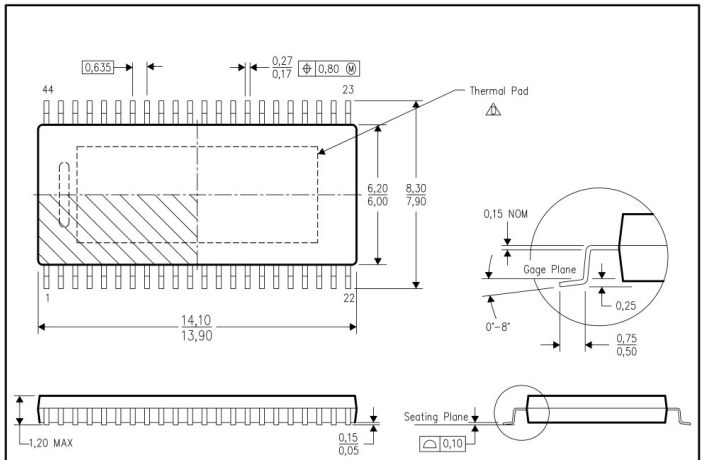
B1: Do not block the heat transfer path at bottom side. Clear as much space as possible for better heat spreading.

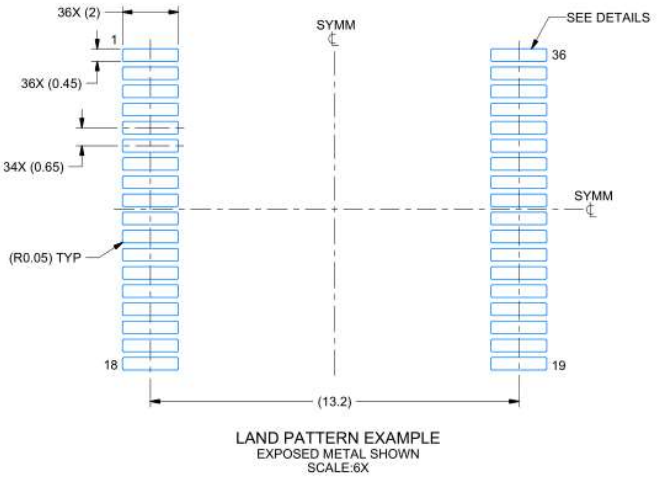
Figure 22. Printed Circuit Board – Bottom Layer



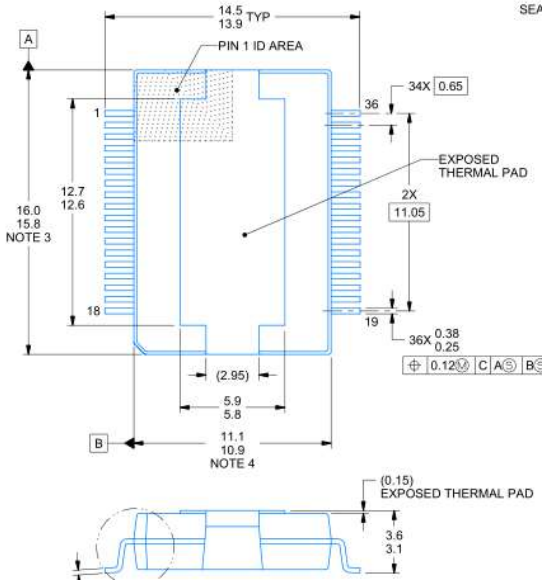
DRV8432

DDW (R–PDSO–G44) PowerPAD ™PLASTIC SMALL–OUTLINE PACKAGE (PAD DOWN)





LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



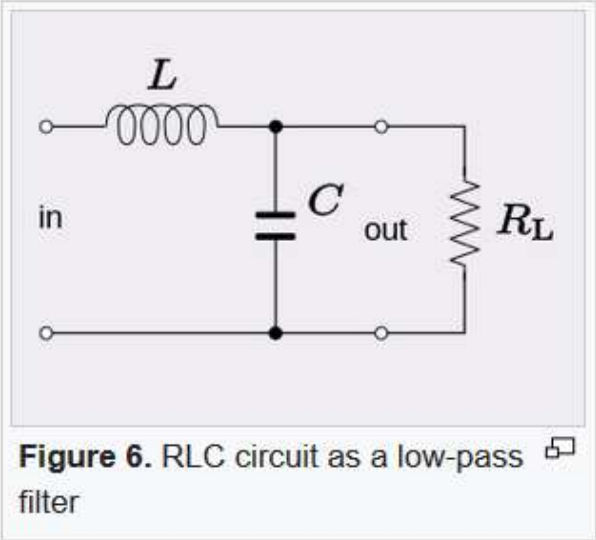


Figure 6. RLC circuit as a low-pass filter

Low-pass filter [edit]

An RLC circuit can be used as a low-pass filter. The circuit configuration is shown in Figure 6. The corner frequency, that is, the frequency of the 3 dB point, is given by

$$\omega_c = \frac{1}{\sqrt{LC}}.$$

This is also the bandwidth of the filter. The damping factor is given by[27]

$$\zeta = \frac{1}{2R_L}\sqrt{\frac{L}{C}}.$$

8.2.4 TEC Driver

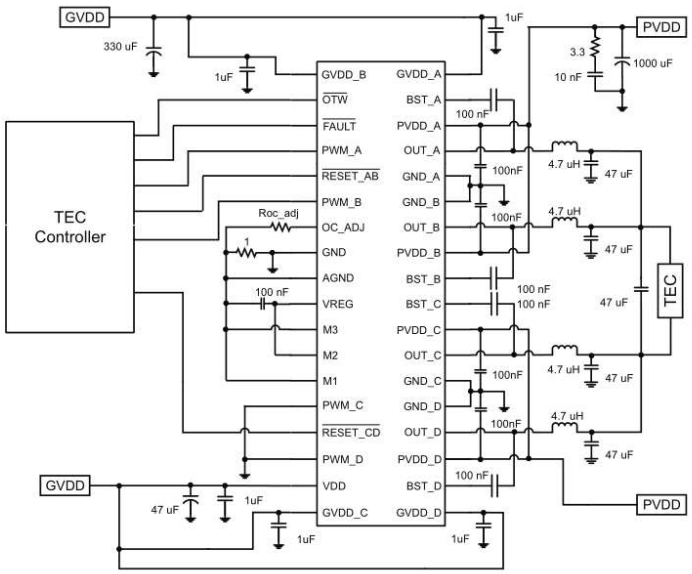
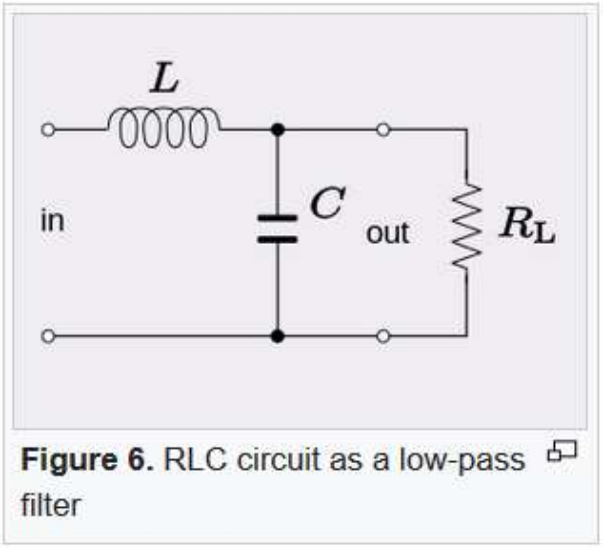


Figure 17. Application Diagram Example for TEC Driver Schematic



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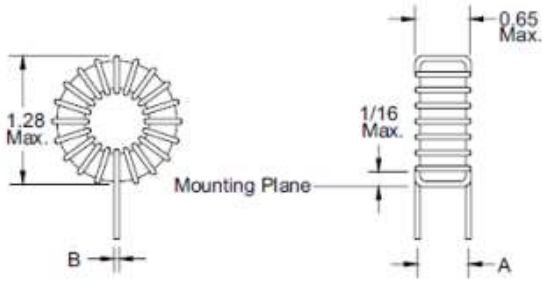
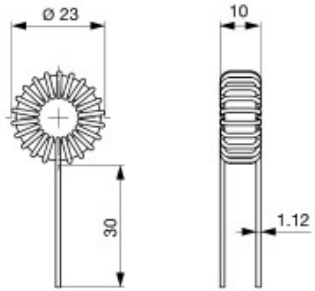
$$\zeta = \frac{1}{2R_L}\sqrt{\frac{L}{C}}.$$

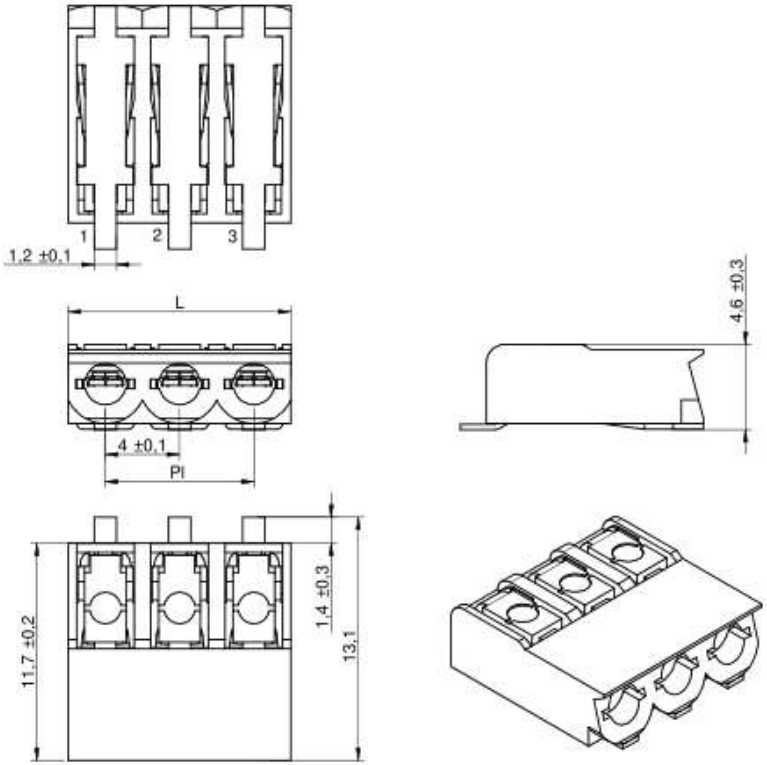


Part Number	L (u H) ±15% @ 1KHz	L(u H) ±15% @ I-rated	DC Resistance Ω MAX	I-rated DC Current Amps (2)	Dimension A (inches) Nominal	Dimension B (inches) Nominal
HCTI-270-5.5	270	147.2	0.060	5.50	0.56	0.042
HCTI-330-5.2	330	174.1	0.067	5.20	0.56	0.042
HCTI-390-5.0	390	200.2	0.072	5.00	0.56	0.042

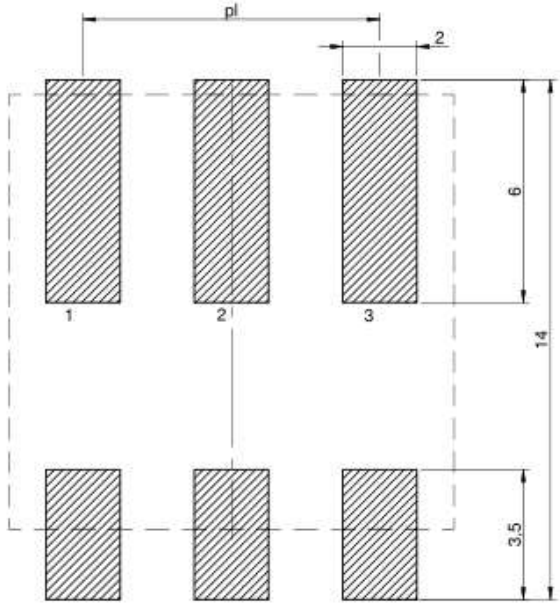
Dimension [mm]
DEN0-23-0001



Dimensions: [mm]



Recommended Land Pattern: [mm]



Pattern Properties:

Properties		Value	Unit
Pin to Pin (Middle)	p_1	4	mm

Article Properties:

Properties		Value	Unit
Pins		2	
Pin to Pin (Middle)	P_1	4	mm
Length	L	8	mm

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eiSos@we-online.com

WÜRTH ELEKTRONIK

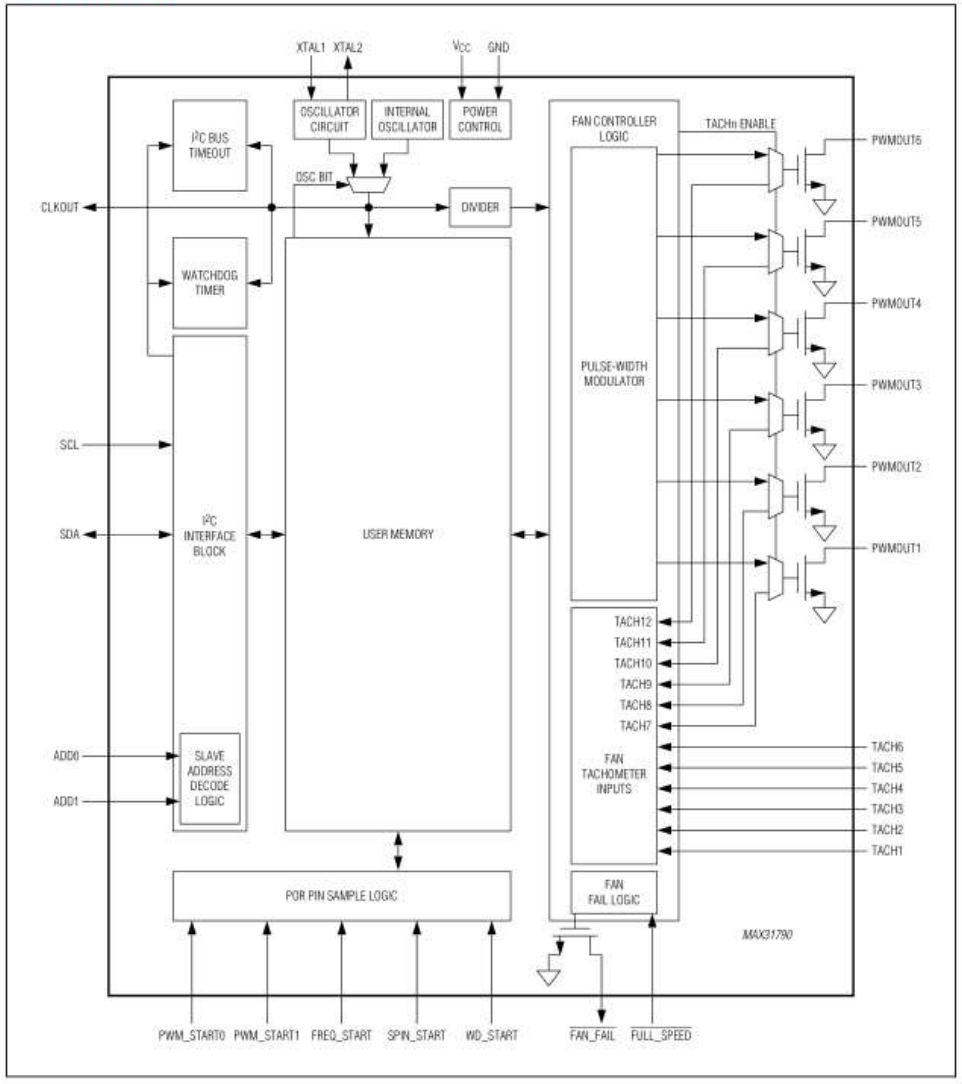
CREATED	CHECKED	GENERAL TOLERANCE	PROJECTION METHOD
WE	WE	DIN ISO 2768-1m	

DESCRIPTION
Serie 400 - 4.00mm SMT Horizontal Entry Connector 4.60mm Height WR-LECO

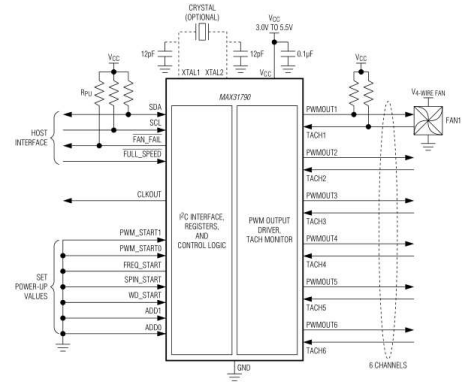
ORDER CODE
695402400222

REVISION	STATUS	DATE (YYYY-MM-DD)	BUSINESS UNIT	PAGE
001.001	Valid	2017-08-07	eiCan	1/5

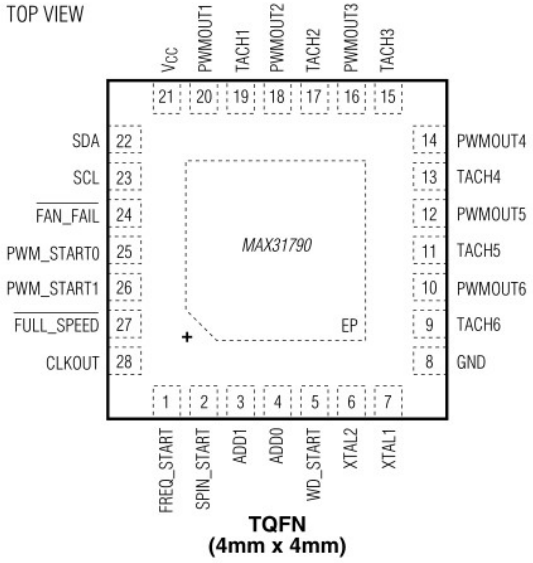
Block Diagram



Typical Operating Circuit



TOP VIEW



TQFN
(4mm x 4mm)

POR Options

Five inputs allow setup of the device's behavior at power-up. The following inputs are sampled when power is first applied to the device:

WD_START: At power-up the watchdog operation is controlled by the WD_START pin. Connect WD_START to V_{CC} to enable, or to GND to disable the watchdog function. When enabled using WD_START, the timeout period is 30s. After power is applied, the watchdog function can be enabled or disabled, and the timeout period can be changed by editing the Global Configuration register.

SPIN_START: At power-up, spin-up operation is controlled by the SPIN_START pin. Connect SPIN_START to GND to disable, V_{CC} to enable spin-up for a maximum of 1s, or unconnected to enable spin-up for a maximum of 0.5s. After power is applied, the spin-up function can be enabled or disabled, and the spin-up period can be changed by editing the associated Fan Configuration register.

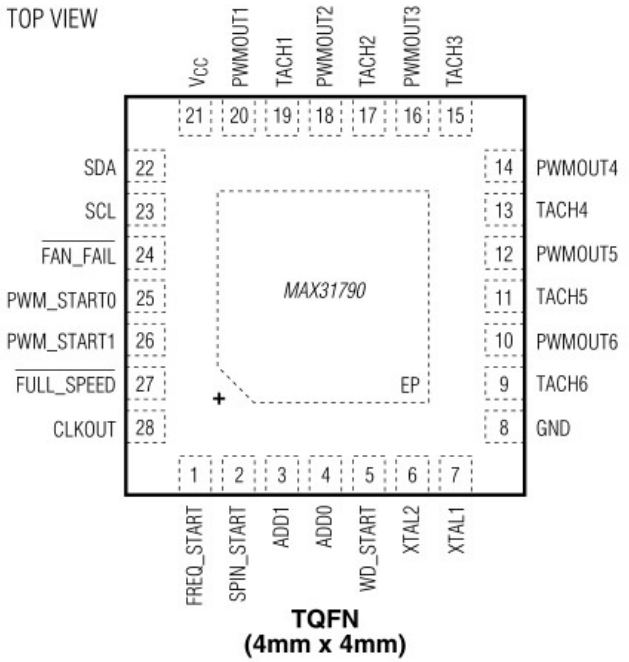
PWM_START0, PWM_START1: At power-up, the PWM output duty cycles are controlled by the PWM_START0 and PWM_START1 pins. Connect PWM_START0/PWM_START1 to GND, V_{CC}, or leave unconnected to achieve different duty cycles for all PWM outputs. See the PWMOUT Target Duty Cycle register for the corresponding values and connections. After power is applied, the PWM duty cycles can be changed, by editing that PWM's associated PWMOUT Target Duty Cycle register.

FREQ_START: At power-up, all PWM output frequencies are controlled by the FREQ_START pin. Connect FREQ_START to GND for 30Hz, V_{CC} for 25kHz, or unconnected for 1.47kHz. After power is applied, the PWM output frequencies can be changed by editing the PWM Frequency register.

Watchdog

The device includes an optional I²C watchdog function that monitors the I²C bus for transactions. When the watchdog function is enabled, all fans (with the exception of failed fans "0% on fail" selected) are forced to full speed if no I²C transactions occur within a selected period (5s, 10s, or 30s). Watchdog timing is selected using the Global Configuration register.

PIN	NAME	FUNCTION
1	FREQ_START	This input is sampled at power-up and sets the power-up value for the PWM output frequency. See the *Register Map* for values.
2	SPIN_START	This input is sampled at power-up and sets the initial spin-up behavior. See the *Register Map* for values.
3	ADD1	Address Select Inputs. Sampled at the start of every I²C transaction. One of 16 possible addresses can be selected by connecting ADD0 and ADD1 to GND, VCC, SDA, or SCL.
4	ADD0	
5	WD_START	This input is sampled at power-up and sets the initial I²C watchdog behavior. See the *Register Map* for values.
6	XTAL2	Pins for Connecting to Optional 32,768Hz Crystal. The crystal can be used when the best RPM precision is required. At POR the internal oscillator is used, and a nominal 32,768Hz clock is produced at CLKOUT. If a crystal is connected between XTAL1 and XTAL2, the crystal oscillator can be enabled by writing to a register. If no crystal is present, ground XTAL1 and leave XTAL2 unconnected.
7	XTAL1	
8	GND	Ground
11	TACH5	Logic/Analog Inputs for Tach Signals. If a fan has a logic tach output, it can be used for RPM control. For a 2-wire fan, analog input can be used for fan-failure detection. Also functions as a “locked rotor” input.
13	TACH4	
15	TACH3	
17	TACH2	
19	TACH1	
10	PWMOUT6	Open-Drain Output to 4-Wire Fan’s PWM Input or (Less Frequently) to Power Transistor Modulating Fan Power Supply. Can also be used as a tachometer signal input. Can be pulled up as high as 5.5V.
12	PWMOUT5	
14	PWMOUT4	
16	PWMOUT3	
18	PWMOUT2	
20	PWMOUT1	
21	VCC	Power-Supply Input. 3.3V nominal. Bypass VCC to GND with a 0.1µF capacitor.
22	SDA	I²C Serial-Data Input/Output, Open Drain. Can be pulled up to 5.5V regardless of VCC.
23	SCL	I²C Serial-Clock Input. Can be pulled up to 5.5V regardless of VCC.
24	$\overline{\text{FAN\_FAIL}}$	Active-Low, Open-Drain Fan-Failure Output. Active only when fault is present.
25	PWM_START0	These inputs are sampled at power-up and set the power-up value for all PWMOUT duty cycles. See the *Register Map* for values.
26	PWM_START1	
27	$\overline{\text{FULL\_SPEED}}$	When low, this input forces all PWM outputs to 100%. Exception: If a fan has failed and “Duty Cycle = 0 on Failure” has been selected for that fan.
28	CLKOUT	CMOS Push-Pull 32,768Hz Clock Output. Signal generated from internal oscillator when external crystal is not used. If a crystal is connected between XTAL1 and XTAL2 and enabled, the crystal oscillator generates the output. Output is always active.
—	EP	Exposed Pad. Connect to GND.



TQFN
(4mm x 4mm)

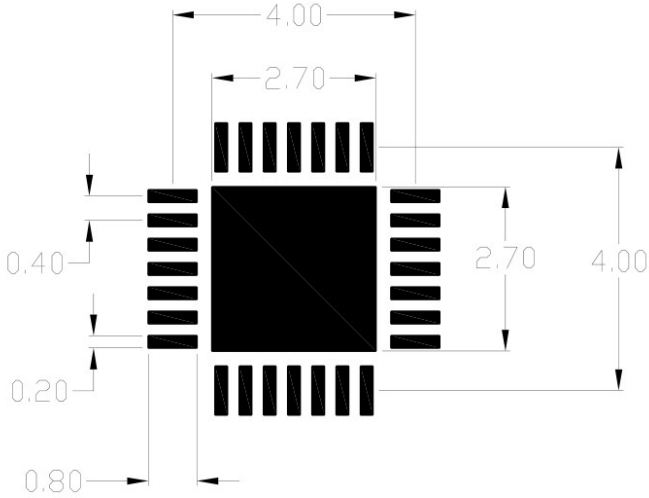


Table 1. Slave Address Table

ADD1 CONNECTION	ADD0 CONNECTION	SLAVE ADDRESS BYTE (HEX)
GND	GND	40
GND	SCL	42
GND	SDA	44
GND	VCC	46
SCL	GND	48
SCL	SCL	4A
SCL	SDA	4C
SCL	VCC	4E
SDA	GND	50
SDA	SCL	52
SDA	SDA	54
SDA	VCC	56
VCC	GND	58
VCC	SCL	5A
VCC	SDA	5C
VCC	VCC	5E

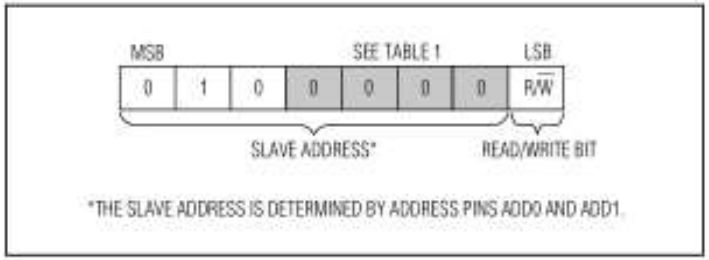
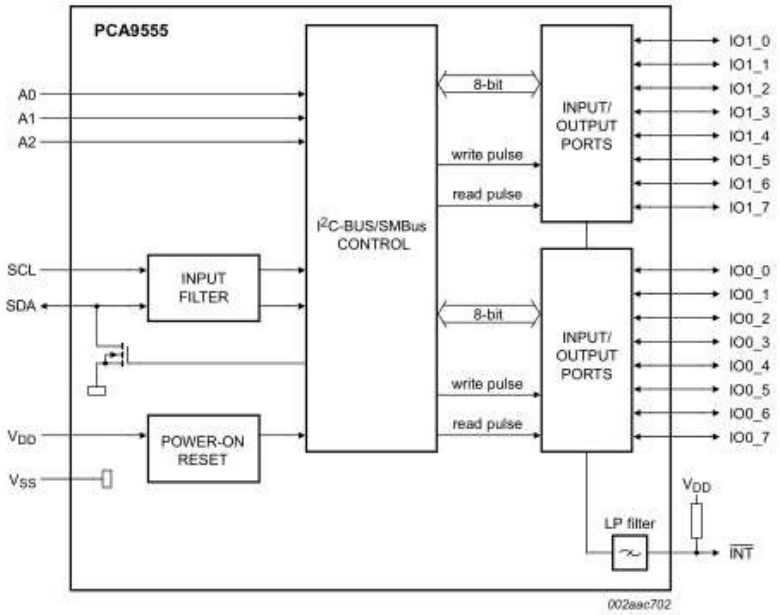


Figure 7. MAX31790 Slave Address Byte Example

BITS 15:7		PWM DUTY CYCLE (%)
DECIMAL	HEX	
0	000h	0
200	0C8h	39
300	12Ch	59
400	190h	78
480	1E0h	94
511	1FFh	100
The value of the PWMOUT target duty cycle at POR depends on the state of the PWM_START0 and PWM_START1 inputs as follows:		
POR CONDITION		
PWM_START0	PWM_START1	PWM DUTY CYCLE (%)
GND	GND	0
GND	Unconnected	30
GND	V_{CC}	40
Unconnected	GND	50
Unconnected	V_{CC}	60
V_{CC}	GND	75
V_{CC}	V_{CC}	100

PCA9555D: I2C GPIO expender, 16 channels

4. Block diagram



Remark: All I/Os are set to inputs at reset.

Fig 1. Block diagram of PCA9555

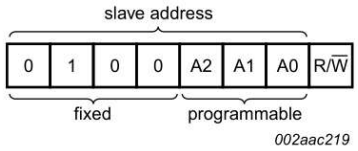


Fig 7. PCA9555 device address

5.1 Pinning

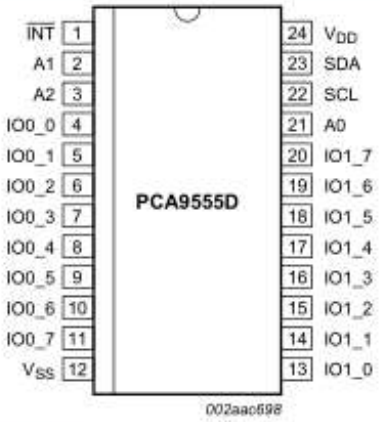
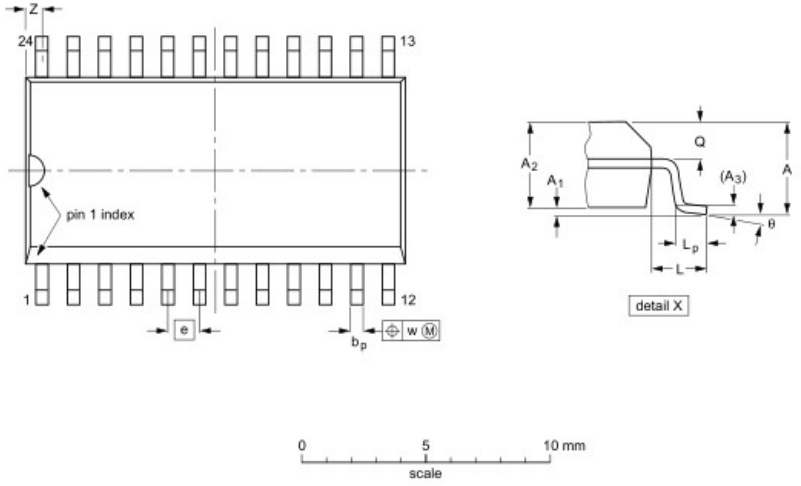


Fig 2. Pin configuration for SO24



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

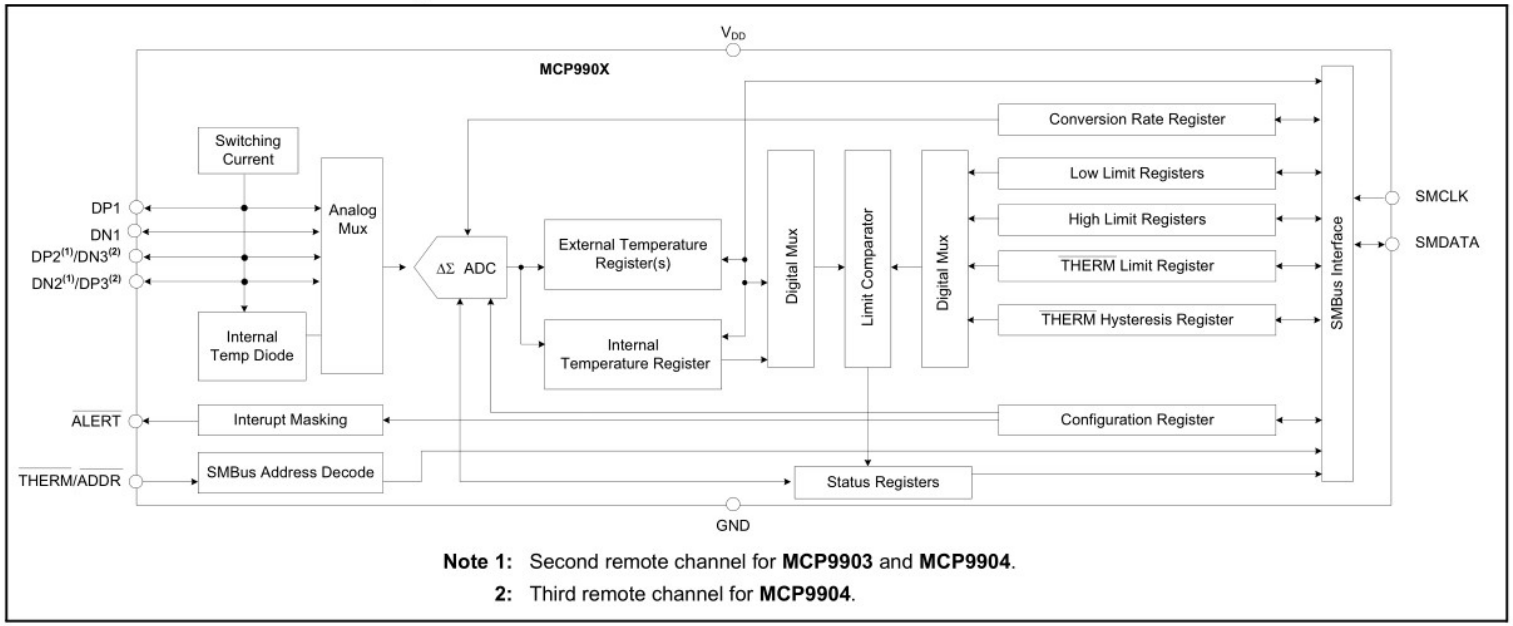
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

https://www.microchip.com/wwwproducts/en/en530196 1.11€/unit

Features

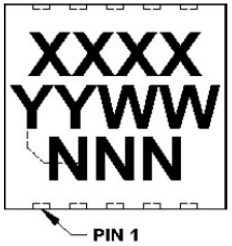
- Up to Three External Temperature Monitors
  - ±1°C maximum accuracy
    MCP9902: -40°C to +105°C
    MCP9903/4: -40°C to +125°C
  - ±2°C maximum accuracy
    (+65°C < T_{DIODE} < +125°C)
  - 0.125°C resolution
- Internal Temperature Monitor
  - ±1°C accuracy
  - (-40°C to +65°C)
  - 0.125°C resolution
- Supports up to 2.2 nF diode filter capacitor
- Up to 400 kHz clock rate
  - Maskable with register control
- Programmable SMBus address
- Operating voltage: 3.0 to 3.6 (V)
- ESD protection: 2 kV HBM
- Temperature Range: -40°C to +125°C
- Available in a small 8-Lead 2x2 mm WDFN and 10-lead 3x3 mm VDFN packages

MCP9902/3/4 Functional Block Diagram



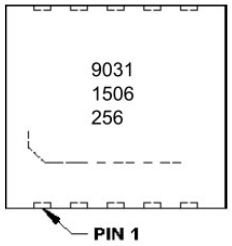
Note 1: Second remote channel for **MCP9903** and **MCP9904**.
2: Third remote channel for **MCP9904**.

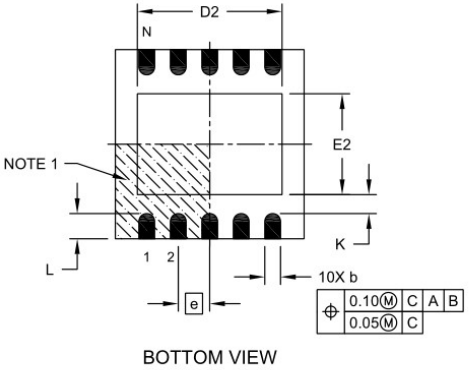
10-Lead VDFN (3 x 3 x 0.9)



Product Number	Code
MCP9903T-1E/9Q	9031
MCP9903T-2E/9Q	9032
MCP9903T-AE/9Q	903A
MCP9904T-1E/9Q	9041
MCP9904T-2E/9Q	9042
MCP9904T-AE/9Q	904A

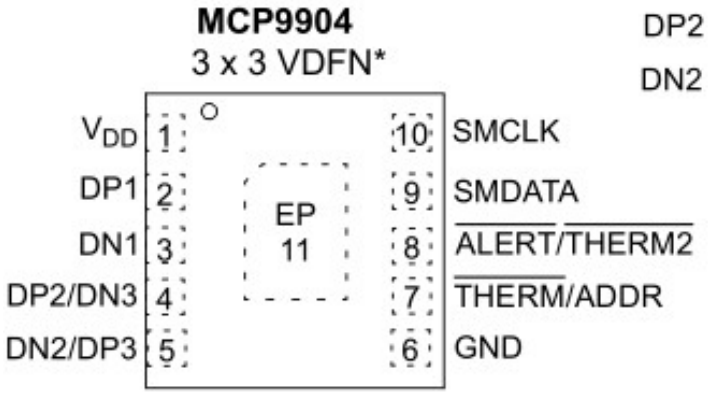
Example





BOTTOM VIEW

Microchip Technology Drawing C04-206A Sheet 1 of 2



MCP9904 VDFN	Pin Name	Pin Type	Description
1	V_{DD}	P	Power
2	DP1	Analog	Diode 1/2 Connection
3	DN1	Analog	Diode 1/2 Connection
4	DP2[1](/DN3)[2]	Analog	Diode 1/2 Connection
5	DN2[1](/DP3)[2]	Analog	Diode 1/2 Connection
6	GND	P	Ground
7	$\overline{\text{THERM}}$/ADDR	OD	Non-Maskable $\overline{\text{THERM}}$
8	$\overline{\text{ALERT}}/\overline{\text{THERM2}}$	OD	Maskable $\overline{\text{ALERT}}/\overline{\text{THERM2}}$
9	SMDATA	OD	SMBus Clock
10	SMCLK	OD	SMBus Data
11	EP	—	Exposed Thermal pad

4.8 Beta Compensation

The MCP9902/3/4 is configured to monitor the temperature of basic diodes (e.g., 2N3904) or CPU

The MCP9904 does not support Beta Compensation on External Diode 2 and External Diode 3 channels due to the high beta of diode-connected transistors.

4.10 Programmable External Diode Ideality Factor

The MCP9902/3/4 is designed for external diodes with an ideality factor of 1.008. Not all external diodes, processor or discrete, will have this exact value. This

3.2 Diode 1 Pair (DN1/DP1)

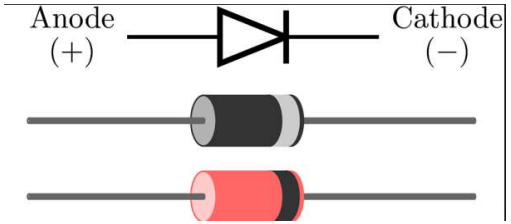
Remote Diode 1 anode (DP1) and cathode (DN1) pins for the MCP9902/3/4.

3.3 Diode 2 Pair (DN2/DP2)

Remote Diode 2 anode (DP2) and cathode (DN2) pins for the MCP9903.

3.4 Anti-Parallel Diode Pair (DN3/DP2 and DN2/DP3) (MCP9904 only)

- DP2/DN3: DP2 anode and DN3 cathode
- DN2/DP3: DN2 cathode and DP3 anode

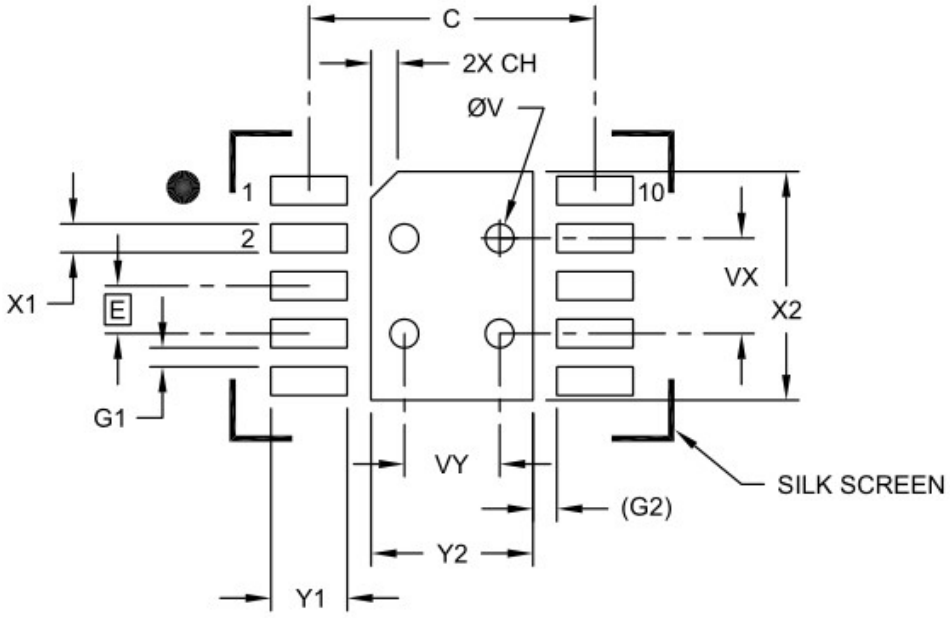


3.5 THERM LIMIT ALERT (THERM/ADDR)

This pin asserts low when the hardware-set THERM limit threshold is exceeded by one of the temperature sensors. The assertion of this signal can't be controlled or masked by register setting. If enabled, the SMBus slave address is set by the pull-up resistor on this pin.

3.10 Exposed Thermal Pad (EP)

Not internally connected, but recommend grounding for mechanical support.



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	Y2			1.70
Optional Center Pad Length	X2			2.40
Contact Pad Spacing	C		3.00	
Center Pad Chamfer	CH		0.28	
Contact Pad Width (X10)	X1			0.30
Contact Pad Length (X10)	Y1			0.80
Contact Pad to Contact Pad (X8)	G1	0.20		
Contact Pad to Center Pad (X10)	G2		0.25 REF	
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	VX		1.00	
Thermal Via Pitch	VY		1.00	

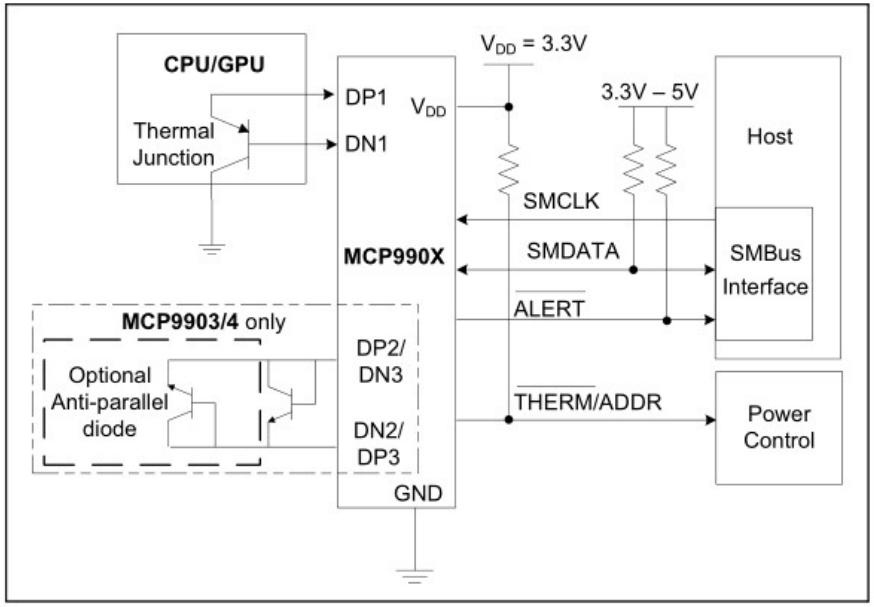


FIGURE 4-1: MCP9902/3/4 *System Diagram.*

4.2 Conversion Rates

The MCP9902/3/4 may be configured for different conversion rates based on the system requirements. The default conversion rate is 4 conversions per second. Other available conversion rates are shown in Table 4-1.

TABLE 4-1: CONVERSION RATE

CONV<3:0>					Conversions/ Second
HEX	3	2	1	0	
0h	0	0	0	0	1/16
1h	0	0	0	1	1/8
2h	0	0	1	0	1/4
3h	0	0	1	1	1/2
4h	0	1	0	0	1
5h	0	1	0	1	2
6h	0	1	1	0	4 (default)
7h	0	1	1	1	8
8h	1	0	0	0	16
9h	1	0	0	1	32
Ah	1	0	1	0	64
Bh - Fh	All others				1

4.3 Dynamic Averaging

TABLE 4-2: I²C/SMBUS ADDRESS DECODE

Pull Up Resistor on THERM pin (±5%)	SMBus Address
4.7 kΩ	1111_100 (r/$\overline{w}$)b
6.8 kΩ	1011_100 (r/$\overline{w}$)b
10 kΩ	1001_100 (r/$\overline{w}$)b
15 kΩ	1101_100 (r/$\overline{w}$)b
22 kΩ	0011_100 (r/$\overline{w}$)b
33 kΩ	0111_100 (r/$\overline{w}$)b

The MCP9902-1 I²C/SMBus address is hard coded to 1001_100(r/$\overline{w}$).

The MCP9902-2 I²C/SMBus address is hard coded to 1001 101(r/$\overline{w}$).

	DRV8830	110 0111	67	Vcc	Open
	DRV8830	110 1000	68	Vcc	Vcc
	MAX31790	010 0000	20	GND	GND
	MAX31790	010 1111	2F	Vcc	Vcc
x	MAX30205	100 1000	48	! A0/A1 depending !	
x	MCP9800_A0	100 1000	48		
	MCP9800_A1	100 1001	49		
	MCP9800_A2	100 1010	4A		
	MCP9800_A3	100 1011	4B		
x	MCP9800_A4	100 1100	4C		
	MCP9800_A5	100 1101	4D		
x	MCP9904-1	1001 100	4C		
	MCP9904	1111 100	7C	4.7k Ohm	
	MCP9904	1011 100	5C	6.8k Ohm	
x	MCP9904	1001 100	4C	10k Ohm	
	MCP9904	1101 100	6C	15k Ohm	
	MCP9904	0011 100	1C	22k Ohm	
	MCP9904	0111 100	3C	33k Ohm	

TABLE 4-7: TEMPERATURE DATA FORMAT

Temperature (°C)	Default Range 0°C to +127°C	Extended Range -64°C to +191°C
Diode Fault	000 0000 0000	000 0000 0000
-64	000 0000 0000	000 0000 0000 (Note 2)
-1	000 0000 0000	001 1111 1000
0	000 0000 0000 (Note 1)	010 0000 0000
0.125	000 0000 0001	010 0000 0001
1	000 0000 1000	010 0000 1000
64	010 0000 0000	100 0000 0000
65	010 0000 1000	100 0000 1000
127	011 1111 1000	101 1111 1000
127.875	011 1111 1111	101 1111 1111
128	011 1111 1111 (Note 3)	110 0000 0000
190	011 1111 1111	111 1111 0000
191	011 1111 1111	111 1111 1000
≥ 191.875	011 1111 1111	111 1111 1111 (Note 4)

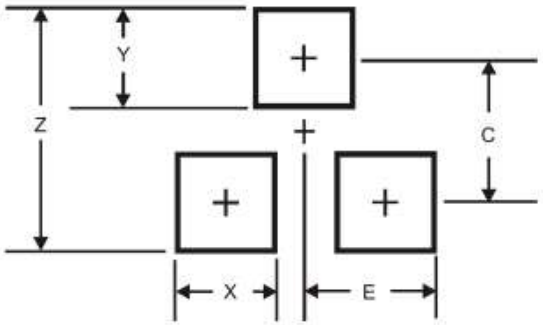
Note 1: In default mode, all temperatures < 0°C will be reported as 0°C

https://www.mouser.fr/ProductDetail/621-MMBT3904T-F

Suggested Pad Layout

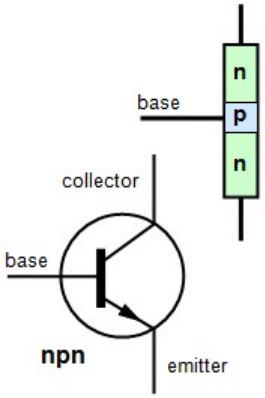
Please see http://www.diodes.com/package-outlines.html for the latest version.

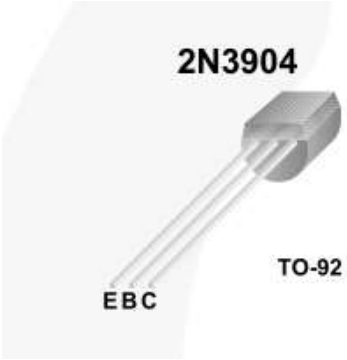
SOT523



Dimensions	Value (in mm)
Z	1.8
X	0.4
Y	0.51
C	1.3
E	0.7

https://www.mouser.fr/ProductDetail/512-2N3904BU





For discrete transistors configured with the collector and base shorted together, the beta is generally sufficiently high such that the percent change in beta variation is very small. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 50 would contribute approximately +0.25°C error at +100°C. However, for substrate transistors where the base-emitter junction is used for temperature measurement and the collector is tied to the substrate, the proportional beta variation will cause large error. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 0.5 would contribute approximately +8.25°C error at +100°C.

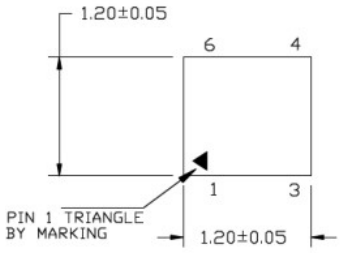
The MCP9904 does not support Beta Compensation on External Diode 2 and External Diode 3 channels due to the high beta of diode-connected transistors.

MIC5528

6-Lead Thin DFN 1.2 mm x 1.2 mm Package Outline and Recommended Land Pattern

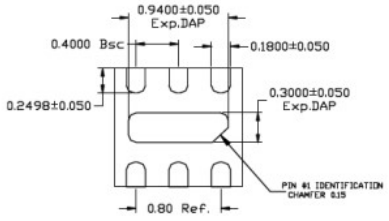
TITLE
6 LEAD TDFN 1.2x1.2mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	TDFN1212-6LD-PL-1	UNIT	MM



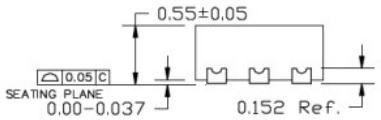
TOP VIEW

NOTE: 1, 2, 3



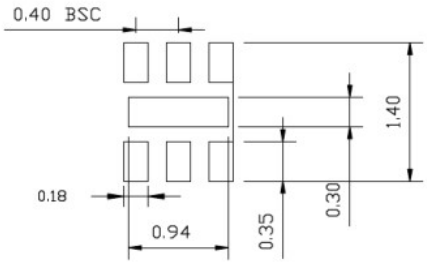
BOTTOM VIEW

NOTE: 1, 2, 3



SIDE VIEW

NOTE: 1, 2, 3



RECOMMENDED LAND PATTERN

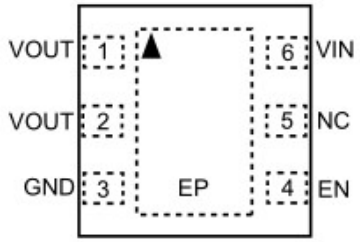
NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED

Features

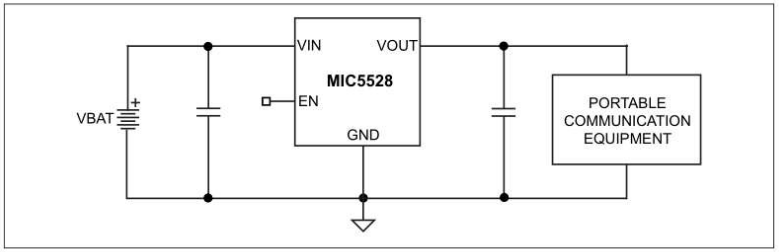
- Input Voltage Range: 2.5V to 5.5V
- Fixed Output Voltages Down to 1.0V
- ±2% Room Temperature Accuracy
- Low Quiescent Current 38 µA
- Stable with 2.2 µF Ceramic Output Capacitors
- Low Dropout Voltage 260 mV @ 500 mA
- Auto-Discharge and Internal Enable Pull-Down
- Thermal Shutdown and Current-Limit Protection
- 6-Pin 1.2 mm × 1.2 mm Extra Thin DFN Package
- 6-Pin 1.2 mm × 1.2 mm Thin DFN Package

Package Types

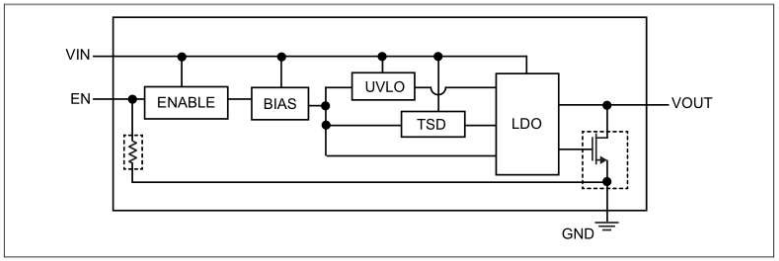
MIC5528
6-Lead Thin DFN (MT)
(Top View)



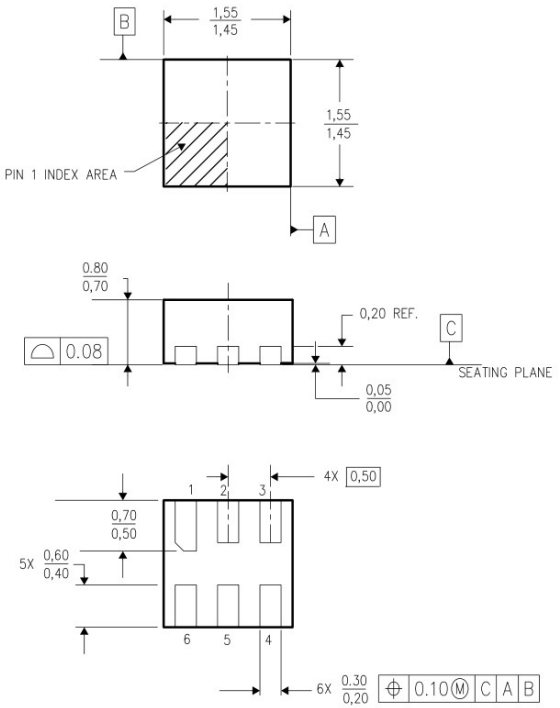
Typical Application Circuit

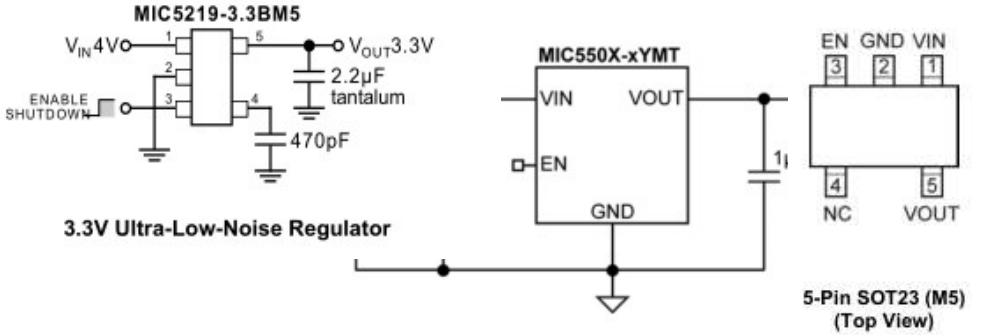


Functional Block Diagram



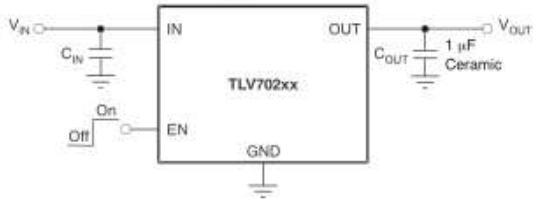
DSE (S–PDSO–N6) PLASTIC SMALL OUTLINE



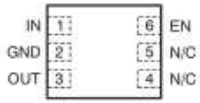


Layout Examples (continued)

Typical Application Circuit



DSE Package
6-Pin WSON
Top View



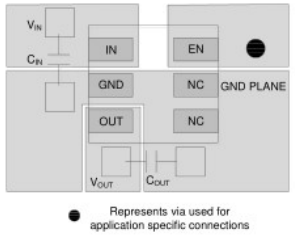


Figure 29. Layout Example for the DSE Package

Table 3. Ordering Information(1)

PRODUCT	V_{OUT} (2)
TLV702**xx** ***yyyz***	**XX** is nominal output voltage (for example, 28 = 2.8 V). **YYY** is the package designator. **Z** is tape and reel quantity (R = 3000, T = 250).

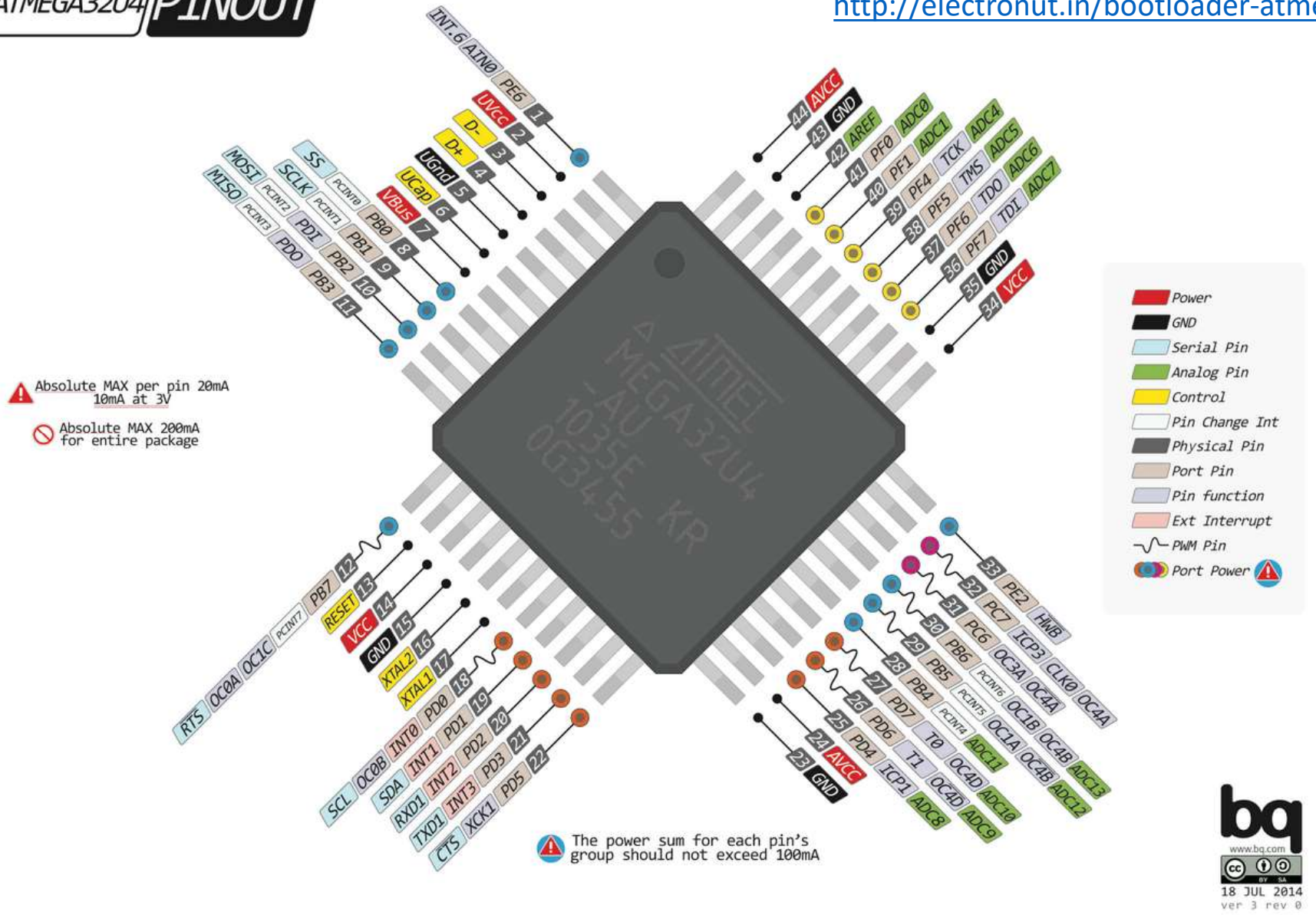
(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.
(2) Output voltages from 1.2 V to 4.8 V in 50-mV increments are available. Contact factory for details and availability.

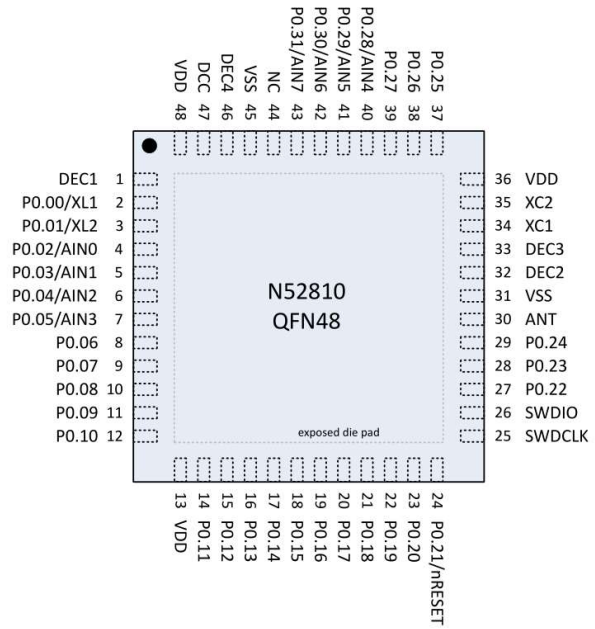
Pin Description

Pin Name	Pin Number Thin DFN-4	Pin Number SOT23-5	Pin Function
VOUT	1	5	Output Voltage. When disabled the MIC5502 and MIC5504 switches in an internal 25Ω load to discharge the external capacitors.
GND	2	2	Ground
EN	3	3	Enable Input: Active High. High = ON; Low = OFF. For MIC5501 and MIC5502 do not leave floating. MIC5503 and MIC5504 have an internal pull-down and this pin may be left floating.
VIN	4	1	Supply Input.
NC	-	4	No Connection. Pin is not internally connected.
ePad	EP	-	Exposed Heatsink Pad. Connect to GND for best thermal performance.

ATMEGA32U4 PINOUT

http://electronut.in/bootloader-atmega32u4/





KEY FEATURES

- Bluetooth 5 ready multi-protocol radio
- Bluetooth 5 datarate support 2Mbps, 1Mbps
- Supports Bluetooth 5 Advertising Extensions
- ARM® Cortex-M4 @ 64MHz
- 192kB flash and 24kB RAM
- Software stacks available as download
- Programmable output power +4dBm to -20dBm
- -96dBm sensitivity for Bluetooth low energy (1Mbps)
- -93dBm sensitivity for Bluetooth 5 (2Mbps)
- On-air compatible with nRF52, nRF51 and nRF24 SoCs
- Supply voltage range
- Programmable Peripheral Interconnect - PPI
- Full range of interfaces SPI/2-wire/UARTE
- High speed SPI 32MHz
- Easy DMA for all digital interfaces
- RAM mapped FIFO using Easy DMA
- 12 bit/200ksps ADC
- On-chip DC-DC buck converter
- Quadrature demodulator
- On-chip balun with 50Ω single-ended output

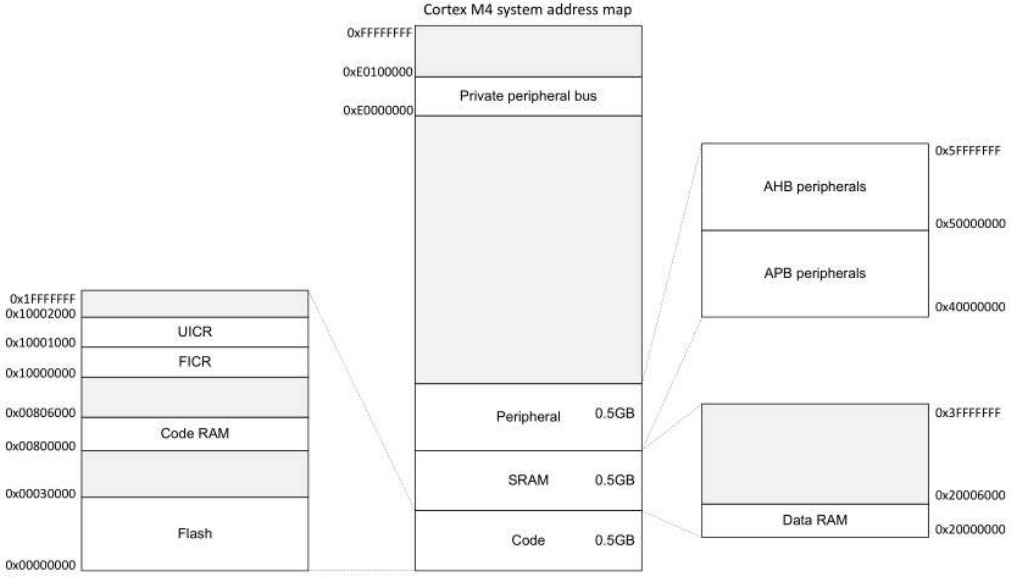


Figure 3: Memory map

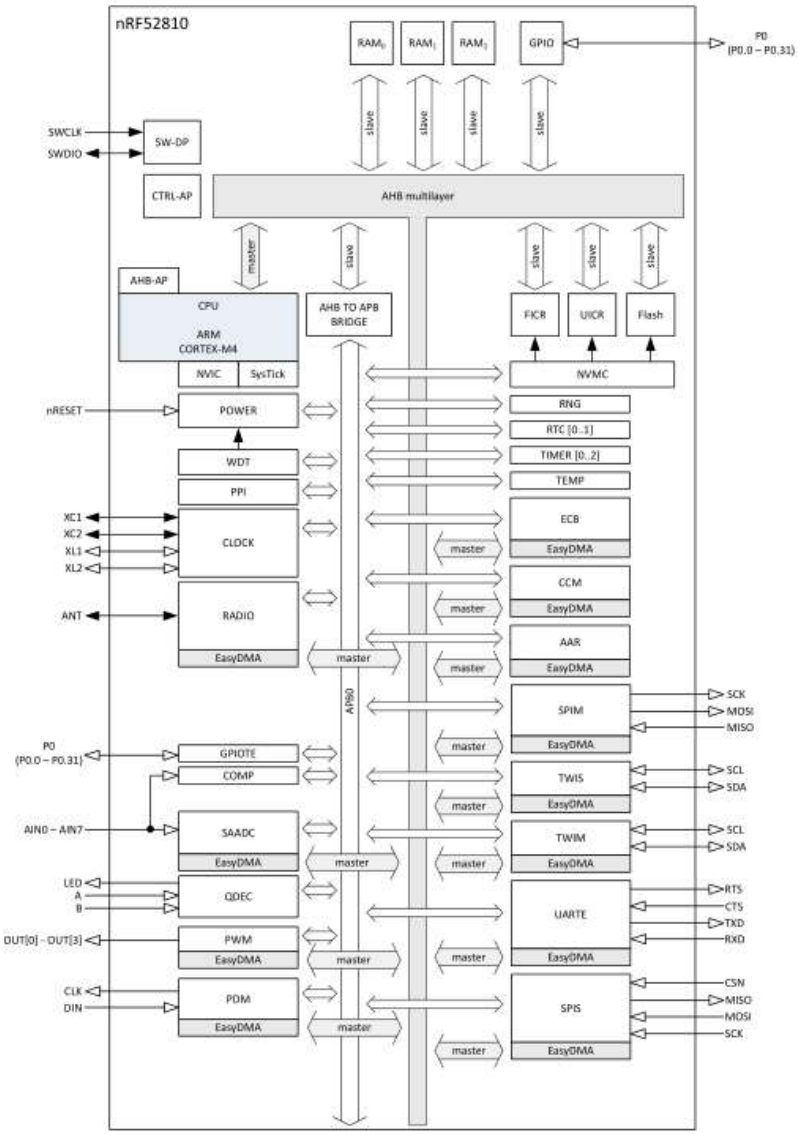
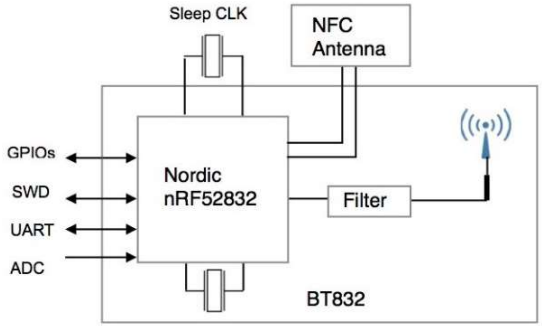


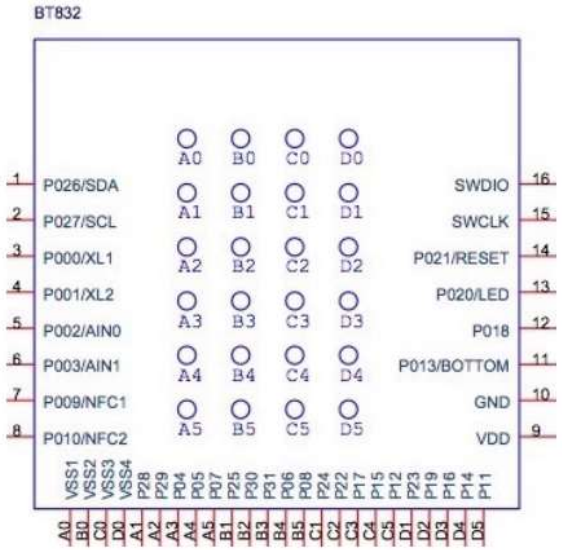
Figure 1: Block diagram

BT832A

- Uses an nRF52810 QFAA with Cortex M4 MCU
- 192 KB flash, 24 KB RAM
- Does not support NFC
- Integrated PCB trace range antenna. Average range is 100 meters. Minimum range and Maximum range around a circle is 75 meters and 140 meters, respectively.
- Size: 14x16x1.9mm.

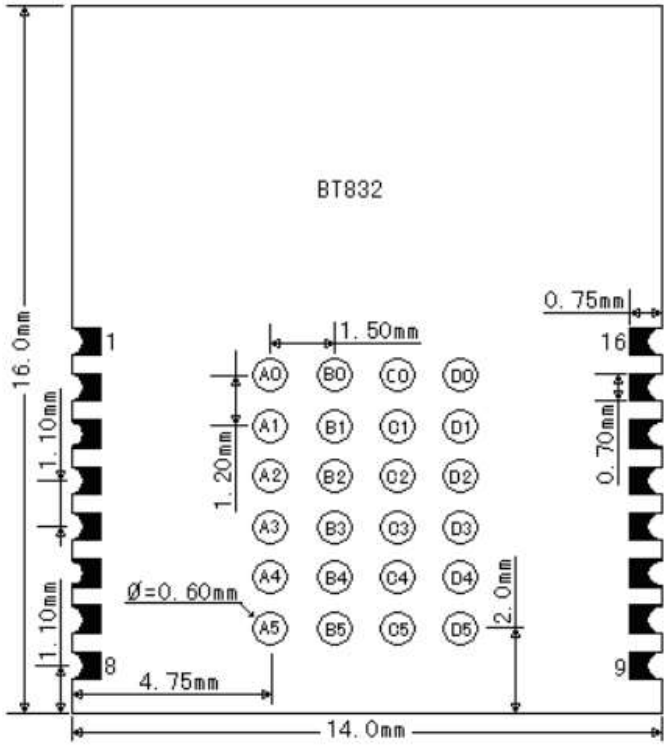


3.8$/unit



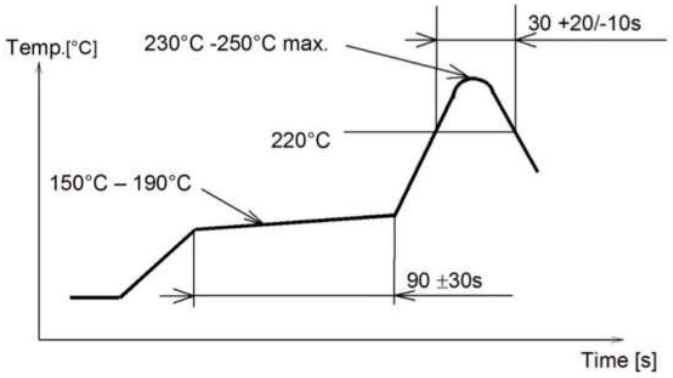
BT832	
pin#	pin name
1	P26/SDA
2	P27/SCL
3	P00/XL1
4	P01/XL2
5	P02/AIN0
6	P03/AIN1
7	P09/NFC1
8	P10/NFC2
9	VDD
10	GND
11	P13
12	P18
13	P20
14	P021/RESET
15	SWDCLK
16	SWDIO
A0	GND

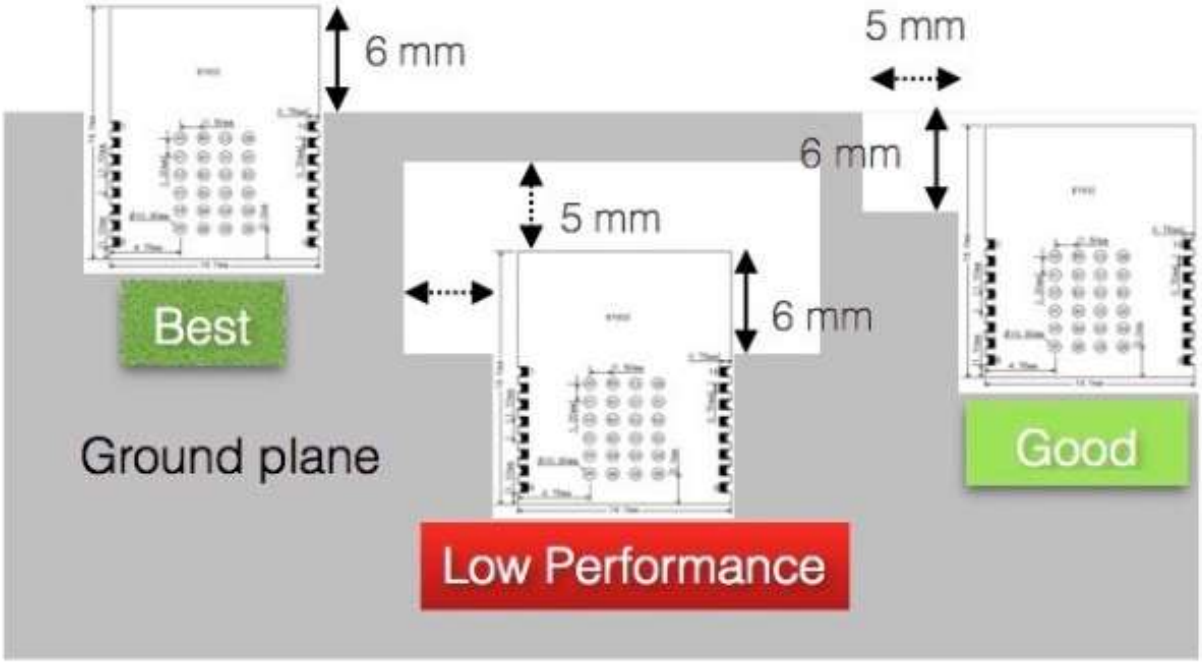
Name	Type	Description
P0.01	Digital I/O	General purpose I/O
XL2	Analog input	Connection for 32.768 kHz crystal (LFXO)
P0.02	Digital I/O	General purpose I/O
AIN0	Analog input	COMP input SAADC input
P0.03	Digital I/O	General purpose I/O
AIN1	Analog input	COMP input
P0.09	Digital I/O	General purpose I/O
P0.10	Digital I/O	General purpose I/O
P0.13	Digital I/O	General purpose I/O
P0.18	Digital I/O	General purpose I/O
P0.20	Digital I/O	General purpose I/O
P0.21	Digital I/O	General purpose I/O
nRESET		Configurable as pin reset
SWDCLK	Digital input	Serial wire debug clock input for debug and programming
SWDIO	Digital I/O	Serial wire debug I/O for debug and programming



Soldering Temperature-Time Profile for Re-Flow Soldering

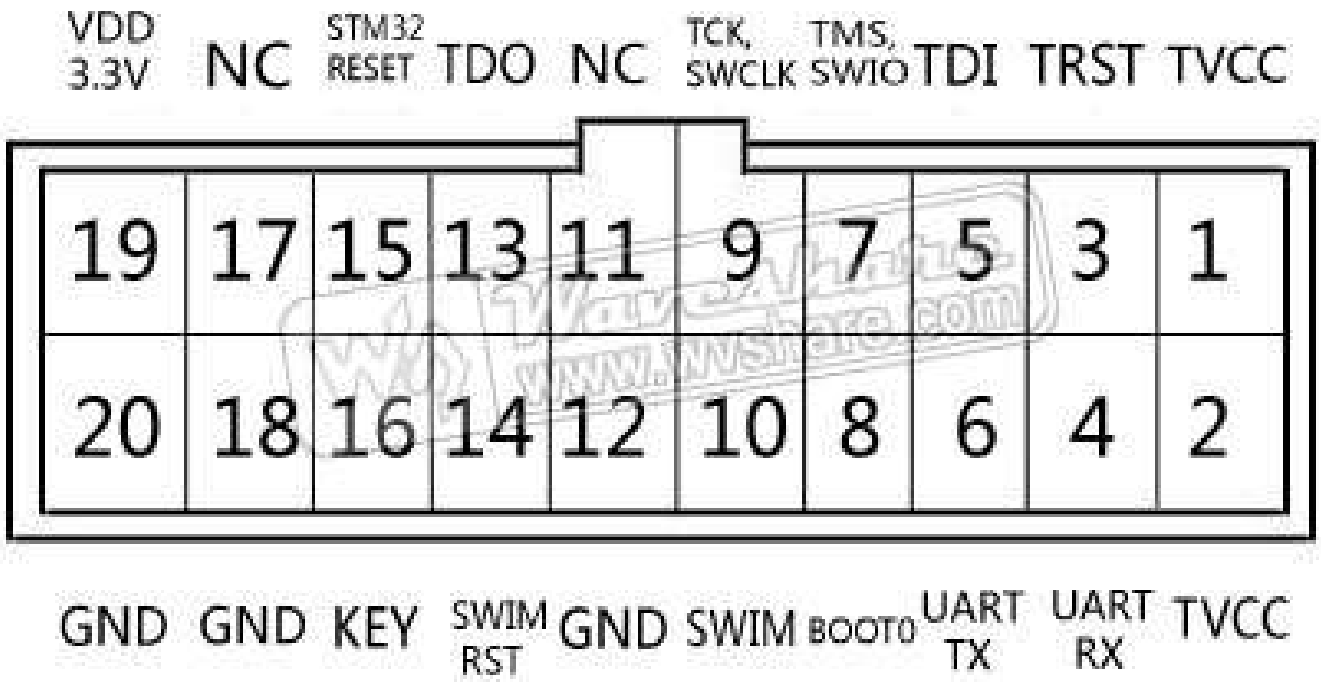
Maximum number of cycles for re-flow is 2. No opposite side re-flow is allowed due to module weight.





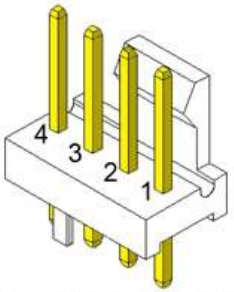
1.BT832 module extends 6 mm from edge or ground plane of the host PCB board.

2.No ground plane on all layers for at least 5mm from edge of module. Longer distance for longer Bluetooth range.



01 Mar 1998

4-Wire Pulse Width Modulation (PWM) Controlled Fans



Motherboard CPU Fan 4 Pin header Connector.

Pin	Name	Color
1	GND	black
2	+12VDC	yellow
3	Sense	green
4	Control	blue

For some AMD cpu fans:

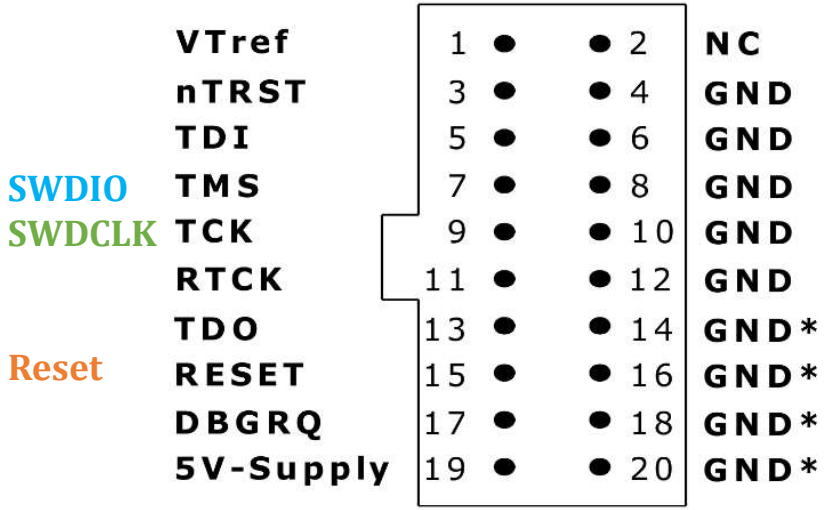
Pin	Name	Color
1	GND	black
2	+12VDC	red
3	Sense	yellow
4	Control	blue

Notes

- Colors may change.

SAM-ICE has a JTAG connector compatible to ARM's Multi-ICE. The JTAG connector is a 20-way Insulation Displacement Connector (IDC) keyed box header (2.54mm male) that mates with IDC sockets mounted on a ribbon cable.

Figure 2-1. JTAG Pinout



The table below lists the SAM-ICE JTAG pinouts.

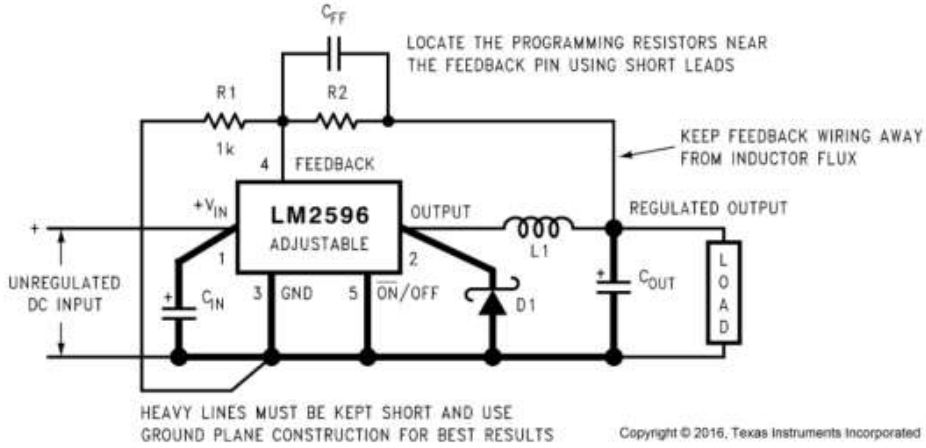
SWD Interface

The SAM-ICE support ARM's Serial Wire Debug (SWD). SWD replaces the 5-pin JTAG port with a clock (SWDCLK) and a single bi-directional data pin (SWDIO), providing all the normal JTAG debug and test functionality. SWDIO and SWCLK are overlaid on the TMS and TCK pins. In order to communicate with a SWD device, J-Link sends out data on SWDIO, synchronous to the SWCLK. With every rising edge of SWCLK, one bit of data is transmitted or received on the SWDIO.

SWD Pinout

The SAM-ICE JTAG connector is also compatible to ARM's Serial Wire Debug (SWD).

9.2.2 LM2596 Adjustable Output Series Buck Regulator



$$V_{OUT} = V_{REF}\left(1 + \frac{R_2}{R_1}\right)$$

where V_{REF} = 1.23 V

$$R_2 = R_1\left(\frac{V_{OUT}}{V_{REF}} - 1\right)$$

Select R_1 to be approximately 1 kΩ, use a 1% resistor for best stability.
C_{IN} — 470-μF, 50-V, Aluminum Electrolytic Nichicon *PL Series*
C_{OUT} — 220-μF, 35-V Aluminum Electrolytic, Nichicon *PL Series*
D1 — 5-A, 40-V Schottky Rectifier, 1N5825
L1 — 68 μH, L38
R1 — 1 kΩ, 1%
C_{FF} — See *Feedforward Capacitor (C_{FF})*