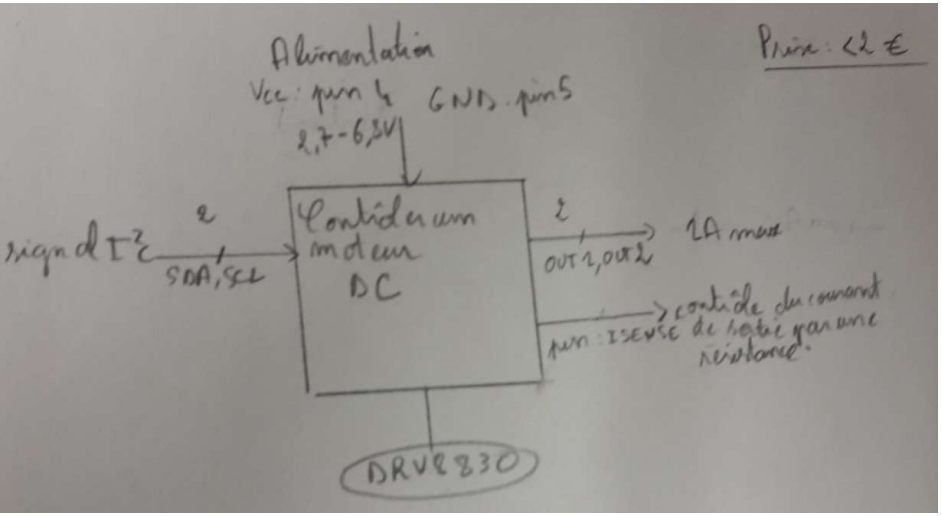
Circuit intégré pour contrôler moteur courant continu: DRV8830



8.2 Typical Application

Figure 11 is a common application of the DRV8830.

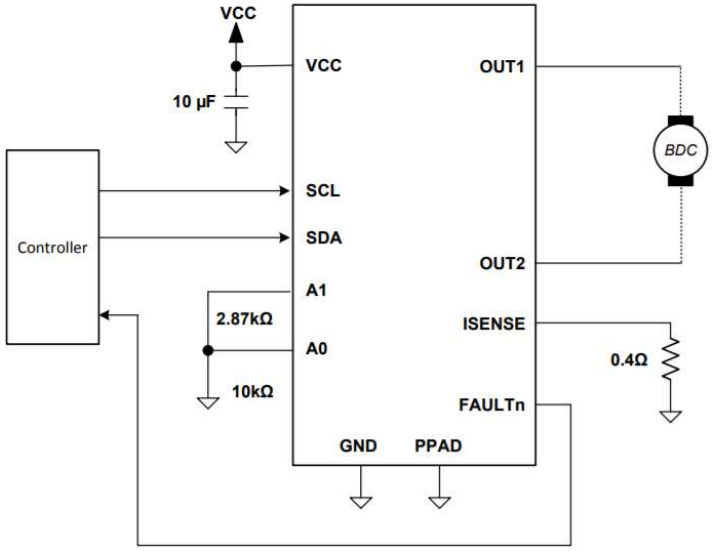
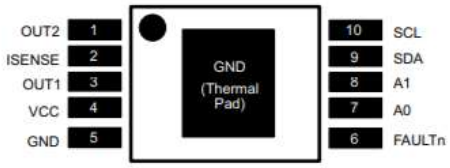


Figure 11. Motor Control Circuitry

DGQ or DRC Package
10-Pin HVSSOP or VSON
Top View



The HVSSOP package has a PowerPAD.

Pin Functions

PIN		TYPE(1)	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NO.			
A0	7	I	Address set 0	Connect to GND, VCC, or open to set I²C base address. See serial interface description.
A1	8	I	Address set 1	
FAULTn	6	OD	Fault output	Open-drain output driven low if fault condition present
GND	5	—	Device ground	
ISENSE	2	IO	Current sense resistor	Connect current sense resistor to GND. Resistor value sets current limit level.
OUT1	3	O	Bridge output 1	Connect to motor winding
OUT2	1	O	Bridge output 2	
SCL	10	I	Serial clock	Clock line of I²C serial bus
SDA	9	IO	Serial data	Data line of I²C serial bus
VCC	4	—	Device and motor supply	Bypass to GND with a 0.1-µF (minimum) ceramic capacitor.

(1) Directions: I = input, O = output, OZ = tri-state output, OD = open-drain output, IO = input/output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
VCC	Power supply voltage	–0.3	7	V
	Input pin voltage	–0.5	7	V
	Peak motor drive output current(3)	Internally limited		A
	Continuous motor drive output current(3)	–1	1	A
	Continuous total power dissipation	See *Thermal Information*		
T_J	Operating virtual junction temperature	–40	150	°C
T_{stg}	Storage temperature	–60	150	

10.2 Layout Example

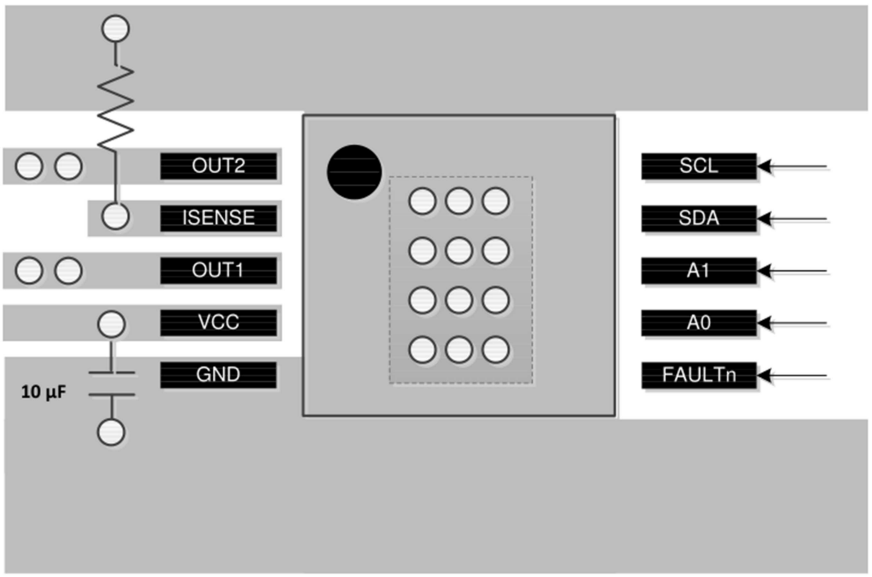
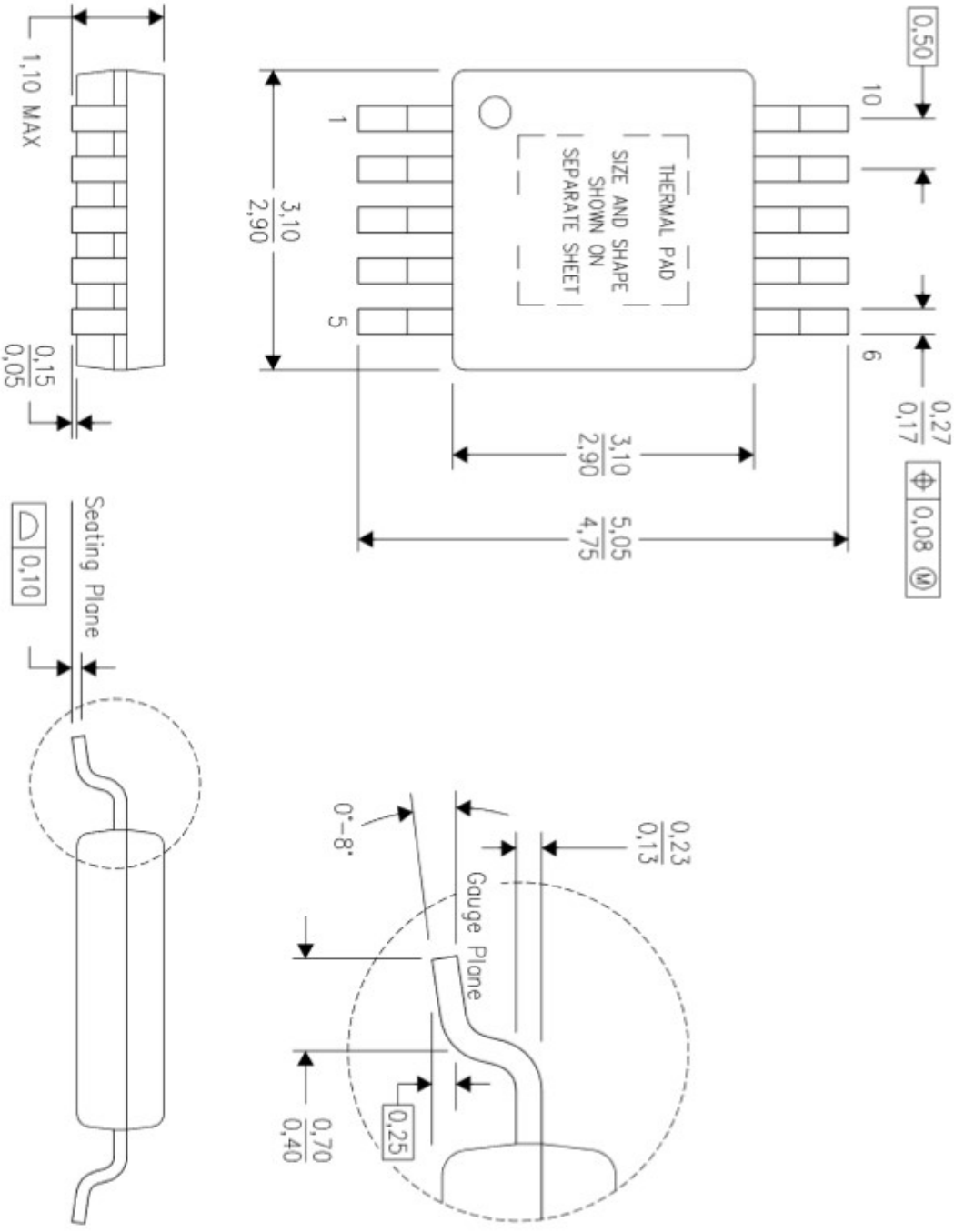
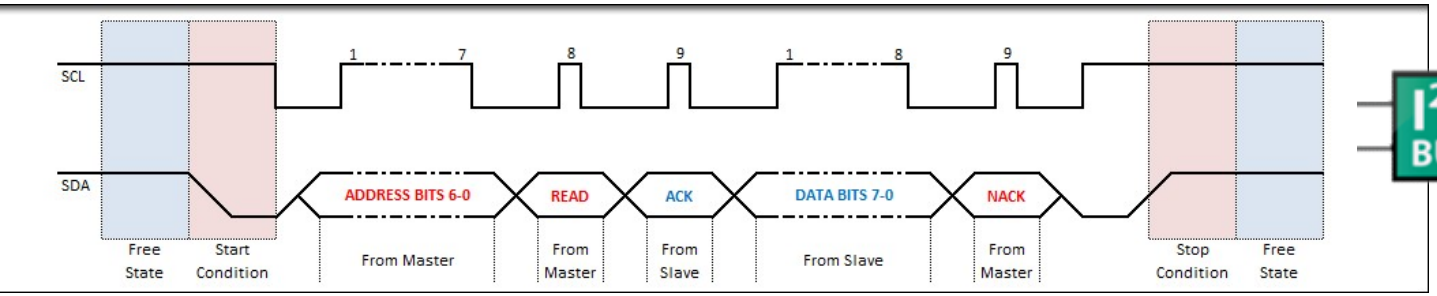
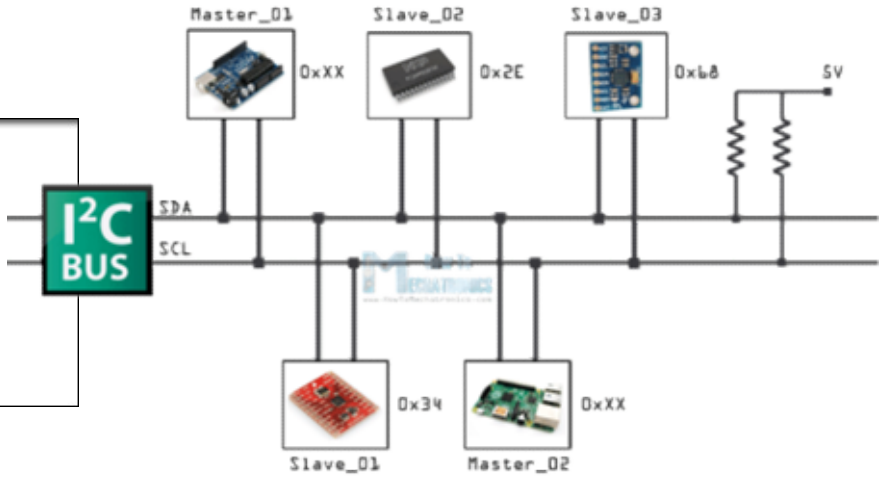


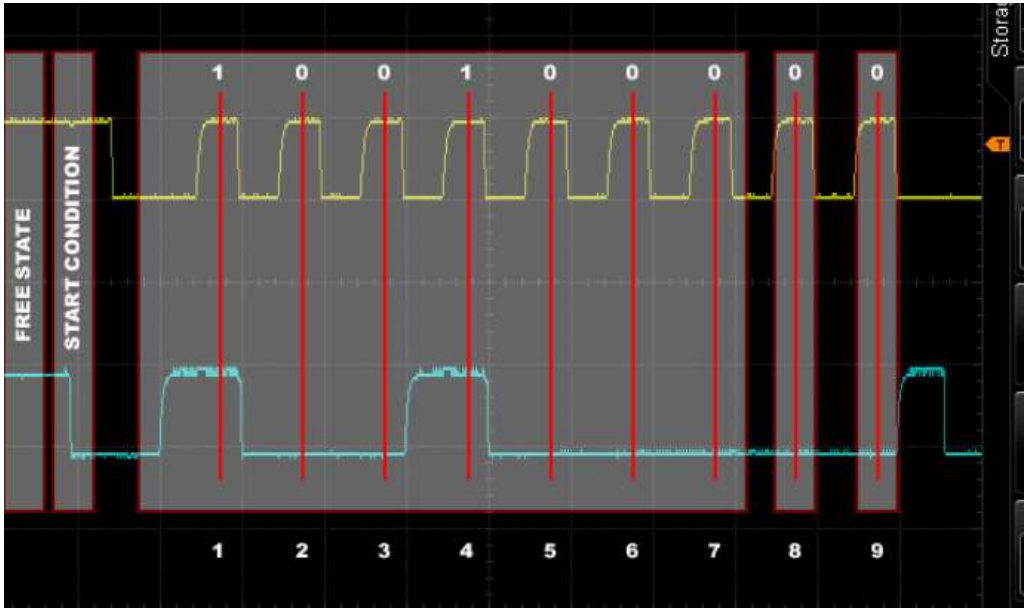
Figure 18. Layout Recommendation



I2C: Two wires for all (as opposed to SPI)







I2C: Two wires for all (as opposed to SPI)

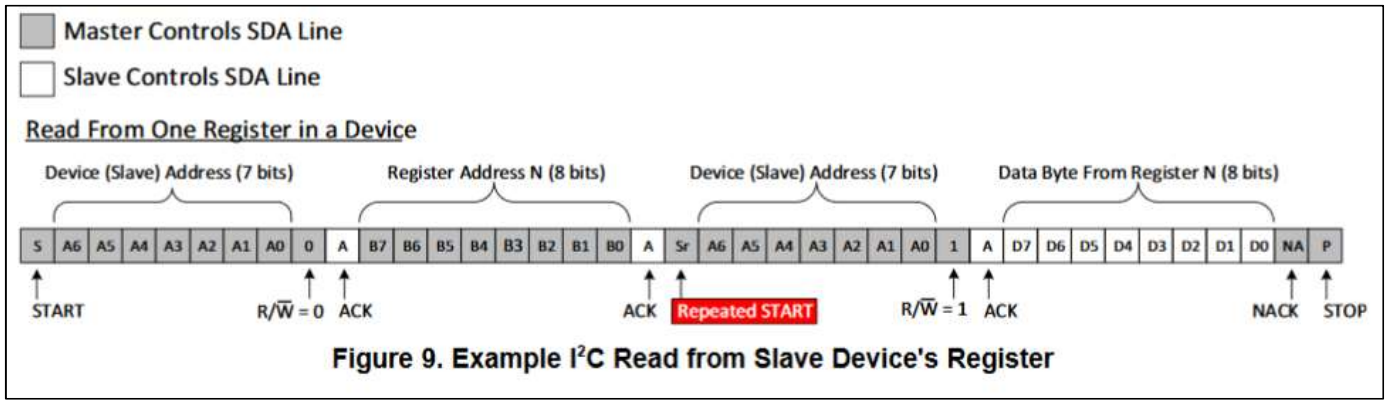


Figure 9. Example I²C Read from Slave Device's Register

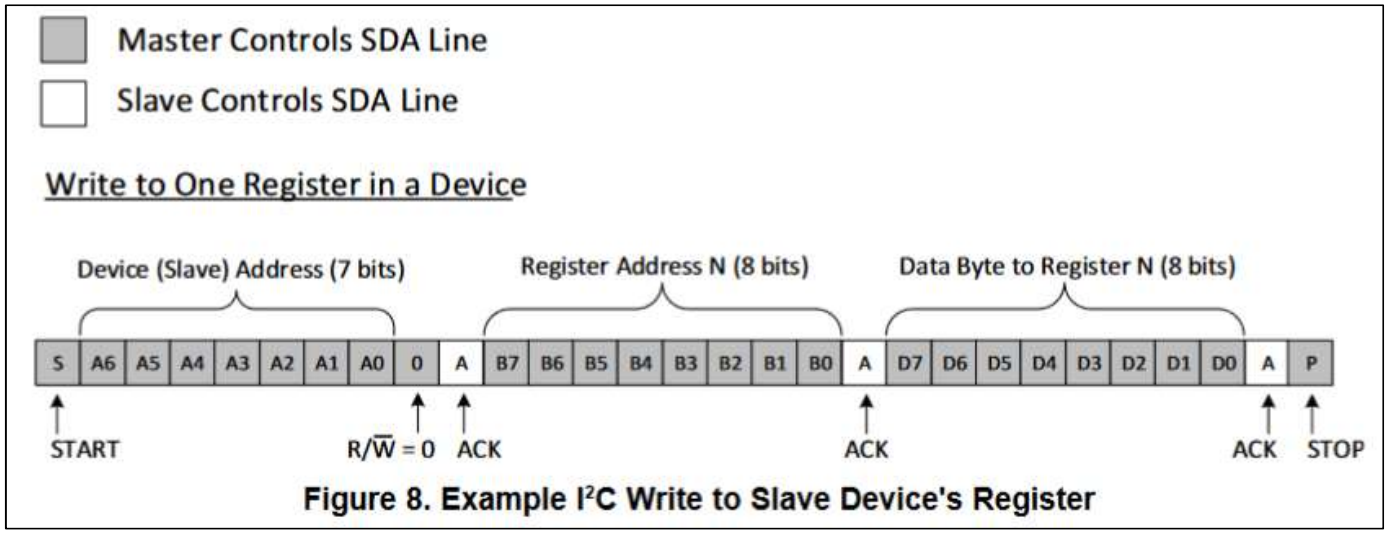


Figure 8. Example I²C Write to Slave Device's Register

ARDUINO

Wire Library

Functions

- begin()
- requestFrom()
- beginTransmission()
- endTransmission()
- write()
- available()
- read()
- SetClock()
- onReceive()
- onRequest()

DRV8830 I2C

The upper address bits of the device address are fixed at 0xC0h, so the device address is as follows:

Table 5. Device Addresses

A1 PIN	A0 PIN	A3..A0 BITS (as below)	ADDRESS (WRITE)	ADDRESS (READ)
0	0	0000	0xC0h	0xC1h
0	open	0001	0xC2h	0xC3h
0	1	0010	0xC4h	0xC5h
open	0	0011	0xC6h	0xC7h
open	open	0100	0xC8h	0xC9h
open	1	0101	0xCAh	0xCBh
1	0	0110	0xCCh	0xCDh
1	open	0111	0xCEh	0xCFh
1	1	1000	0xD0h	0xD1h

The DRV8830 does not respond to the general call address.

A data byte follows the address acknowledge. If the R/W bit is low, the data is written from the master. If the R/W bit is high, the data from this device are the values read from the register previously selected by a write to the subaddress register. The data byte is followed by an acknowledge sent from this device. Data is output only if

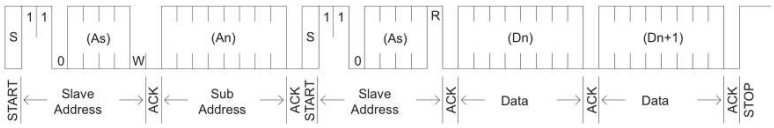


Figure 9. I²C Read Mode

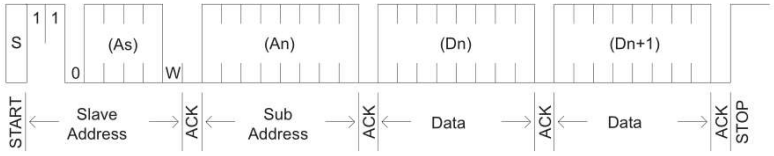


Figure 10. I²C Write Mode

7.6 Register Maps

7.6.1 I²C Register Map

Table 6. I²C Register Map

REGISTER	SUB ADDRESS (HEX)	REGISTER NAME	DEFAULT VALUE	DESCRIPTION
0	0x00	CONTROL	0x00h	Sets state of outputs and output voltage
1	0x01	FAULT	0x00h	Allows reading and clearing of fault conditions

7.6.1.1 REGISTER 0 – CONTROL

The CONTROL register is used to set the state of the outputs as well as the DAC setting for the output voltage. The register is defined as follows:

Table 7. Register 0 – Control

D7 - D2	D1	D0
VSET[5..0]	IN2	IN1

Table 4. H-Bridge Logic

IN1	IN2	OUT1	OUT2	FUNCTION
0	0	Z	Z	Standby / coast
0	1	L	H	Reverse
1	0	H	L	Forward
1	1	H	H	Brake

VSET[5..0]: Sets DAC output voltage. Refer to V

IN2: Along with IN1, sets state of outputs

IN1: Along with IN2, sets state of outputs

Table 1. Commanded Output Voltage (continued)

VSET[5..0]	OUTPUT VOLTAGE	VSET[5..0]	OUTPUT VOLTAGE
0x10h	1.29	0x30h	3.86
0x11h	1.37	0x31h	3.94
0x12h	1.45	0x32h	4.02

7.6.1.2 REGISTER 1 – FAULT

The FAULT register is used to read the source of a fault condition, and to clear the status bits that indicated the fault. The register is defined as follows:

Table 8. Register 1 – Fault

D7	D6 - D5	D4	D3	D2	D1	D0
CLEAR	Unused	ILIMIT	OTS	UVLO	OCP	FAULT

CLEAR: When written to 1, clears the fault status bits

ILIMIT: If set, indicates the fault was caused by an extended current limit event

OTS: If set, indicates that the fault was caused by an overtemperature (OTS) condition

UVLO: If set, indicates the fault was caused by an undervoltage lockout

OCP: If set, indicates the fault was caused by an overcurrent (OCP) event

FAULT: Set if any fault condition exists